Bachelor of Technology - Electronics & Communication Engineering

Syllabus - First Semester

INTRODUCTION TO COMPUTERS AND PROGRAMMING IN C

Course Code: ECE2105 **CreditUnits: 03**

Course Objective:
The objective of this course module is to acquaint the students with the basics of computers system, its components, data representation inside computer and to get them familiar with various important features of procedure oriented programming language i.e. C.

Course Contents:
Module I: Introduction
Introduction to computer, history, von-Neumann architecture, memory system (hierarchy, characteristics and types), H/W concepts (I/O Devices), S/W concepts (System S/W & Application S/W, utilities). Data Representation: Number systems, character representation codes, Binary, octal, hexadecimal and their interconversions. Binary arithmetic, floating point arithmetic, signed and unsigned numbers, Memory storage unit.

Module II: Programming in C
History of C, Introduction of C, Basic structure of C program, Concept of variables, constants and data types in C, Operators and expressions: Introduction, arithmetic, relational, Logical, Assignment, Increment and decrement operator, Conditional, bitwise operators, Expressions, Operator precedence and associativity. Managing Input and output Operation, formatting I/O.

Module III: Fundamental Features in C
C Statements, conditional executing using if, else, nesting of if, switch and break Concepts of loops, example of loops in C using for, while and do-while, continue and break. Storage types (automatic, register etc.), predefined processor, Command Line Argument.

Module IV: Arrays and Functions
One dimensional arrays and example of iterative programs using arrays, 2-D arrays Use in matrix computations.
Concept of Sub-programming, functions Example of user defined functions. Function prototype, Return values and their types, calling function, function argument, function with variable number of argument, recursion.

Module V: Advanced features in C
Pointers, relationship between arrays and pointers Argument passing using pointers, Array of pointers. Passing arrays as arguments.
Strings and C string library.
Structure and Union. Defining C structures, Giving values to members, Array of structure, Nested structure, passing strings as arguments.
File Handling.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:

- “ANSI C” by E Balagurusamy
- YashwantKanetkar, “Let us C”, BPB Publications, 2nd Edition, 2001.
- Herbert Schildt, “C: The complete reference”, Osbourne Mcgraw Hill, 4th Edition, 2002.
- V. Raja Raman, “Computer Programming in C”, Prentice Hall of India, 1995.

References:

- Kernighan & Ritchie, “C Programming Language”, The (Ansi C Version), PHI, 2nd Edition.
- J. B Dixit, “Fundamentals of Computers and Programming in ‘C’.
- P.K. Sinha and Priti Sinha, “Computer Fundamentals”, BPB publication.

PROGRAMMING IN C LAB

Course Code: ECE2110 **CreditUnits: 01**

Software Required: Turbo C

Course Contents:

- C program involving problems like finding the nth value of cosine series, Fibonacci series. Etc.
- C programs including user defined function calls
- C programs involving pointers, and solving various problems with the help of those.
- File handling

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

Syllabus - Second Semester

OBJECT ORIENTED PROGRAMMING USING C++

Course Code: ECE2203 **CreditUnits: 03**

Course Objective:
The objective of this module is to introduce object oriented programming. To explore and implement the various features of OOP such as inheritance, polymorphism, Exceptional handling using programming language C++. After completing this course student can easily identify the basic difference between the programming approaches like procedural and object oriented.

Course Contents:
Module I: Introduction
Review of C, Difference between C and C++, Procedure Oriented and Object Oriented Approach. Basic Concepts: Objects, classes, Principals like Abstraction, Encapsulation, Inheritance and Polymorphism. Dynamic Binding, Message Passing. Characteristics of Object-Oriented Languages. Introduction to Object-Oriented Modeling techniques (Object, Functional and Dynamic Modeling).

Module II: Classes and Objects
Abstract data types, Object & classes, attributes, methods, C++ class declaration, Local Class and Global Class, State identity and behaviour of an object, Local Object and Global Object, Scope resolution operator, Friend Functions, Inline functions, Constructors and destructors, instantiation of objects, Types of Constructors, Static Class Data, Array of Objects, Constant member functions and Objects, Memory management Operators.

Module III: Inheritance
Inheritance, Types of Inheritance, access modes – public, private & protected, Abstract Classes, Ambiguity resolution using scope resolution operator and Virtual base class, Aggregation, composition vs classification hiérarchies, Overriding inheritance methods, Constructors in derived classes, Nesting of Classes.

Module IV: Polymorphism
Polymorphism, Type of Polymorphism – Compile time and runtime, Function Overloading, Operator Overloading (Unary and Binary) Polymorphism by parameter, Pointer to objects, this pointer, Virtual Functions, pure virtual functions.

Module V: Strings, Files and Exception Handling
Manipulating strings, Streams and files handling, formatted and Unformatted Input output. Exception handling, Generic Programming – function template, class Template Standard Template Library: Standard Template Library, Overview of Standard Template Library, Containers, Algorithms, Iterators, Other STL Elements, The Container Classes, General Theory of Operation, Vectors.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

Text & References:
Text:

- A.R. Venugopal, Rajkumar, T. Ravishanker "Mastering C++", TMH, 1997
- R. Lafore, "Object Oriented Programming using C++", BPB Publications, 2004.
- "Object Oriented Programming with C++" By E. Balagurusamy.
- Schildt Herbert, "C++: The Complete Reference", Wiley DreamTech, 2005.

References:

- Parasons, "Object Oriented Programming with C++", BPB Publication, 1999.
- Steven C. Lawlor, "The Art of Programming Computer Science with C++", Vikas Publication, 2002.
- YashwantKanethkar, "Object Oriented Programming using C++", BPB, 2004

OBJECT ORIENTED PROGRAMMING USING C++ LAB

Course Code: ECE2206 **CreditUnits: 01**

Software Required: Turbo C++

Course Contents:

- Creation of objects in programs and solving problems through them.
- Different use of private, public member variables and functions and friend functions.
- Use of constructors and destructors.
- Operator overloading
- Use of inheritance in and accessing objects of different derived classes.
- Polymorphism and virtual functions (using pointers).
- File handling.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab

Syllabus - Third Semester

ANALOG ELECTRONICS-I

Course Code: ECE2302 **CreditUnits: 03**

Course Objective:
This course builds from basic knowledge of Semiconductor Physics to an understanding of basic devices and their models. This course builds a foundation for courses on VLSI design and analog CMOS IC Design.

Course Contents:
Module I: Semiconductor Diode and Diode Circuits
Different types of diodes: Zener, Schottky, LED. Zener as voltage regulator, Diffusion capacitance, Drift capacitance, the load line concept, half wave, full wave rectifiers, clipping and clamping circuits.

Module II: Bipolar Junction Transistor
Bipolar junction transistor: Introduction, Transistor, construction, transistor operations, BJT characteristics, load line, operating point, leakage currents, saturation and cut off mode of operations. Bias stabilization: Need for stabilization, fixed Bias, emitter bias, self bias, bias stability with respect to variations in $I_{co,}$ V_{BE} &β, Stabilization factors, thermal stability.

Module III: Small signal Analysis of transistor and Multistage Amplifier
Hybrid model for transistors at low frequencies, Analysis of transistor amplifier using h parameters, emitter follower, Miller's theorem, THE CE amplifier with an emitter resistance, Hybrid π model, Hybrid π Conducatnces and Capacitances, CE short circuit current gain, CE short circuit current gain with R_L Multistage amplifier: Cascading of Amplifiers, Coupling schemes(RC coupling and Transformer coupling)

Module IV: Field Effect Transistors
Field effect transistor (JFET, MOSFET): volt-ampere characteristics, small signal model –common drain, common source, common gate, operating point, MOSFET, enhancement and -depletion mode, Common source amplifier, Source follower

Module V: Feedback Amplifiers
Feedback concept, Classification of Feedback amplifiers, Properties of negative Feedback amplifiers, Impedance considerations in different Configurations, Examples of analysis of feedback Amplifiers.

Module VI: Power amplifiers
Power dissipation in transistors, difference with voltage amplifiers, Amplifier classification (Class A, Class B, Class C, Class AB) class AB push pull amplifier, collector efficiency of each, cross over distortion.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

- Robert F. Pierret: Semiconductor Device Fundamentals, Pearson Education.
- Millman and Halkias: Electronic Devices and circuits, Tata McGraw.
- Boylestad: Electronic Devices and Circuits, Pearson Education.

CIRCUITS & SYSTEMS

Course Code: ECE2303 **CreditUnits: 03**

Course Objective:
The course intends to make the students proficient in analyzing circuits. At the completion of the course, the student should be able to construct and interpret block diagrams and signal flow graphs of control systems and to use basic methods of determining their stability.

Course Contents:

Module I: Graph Theory and Network equations
Graph of a network, Trees, Co-trees and loops, Cut set matrix, Tie set matrix, number of possible trees of a graph, duality, Loop Analysis and Node Analysis.

Module II: Analysis of circuits using classical Method
Time and Frequency domain analysis of RL, RC and RLC circuits, Linear constant coefficient differential equation.

Module III: Signals and Laplace Transforms
Unit step signal, Ramp signal, impulse signal, Laplace transformations and its properties, Gate function, Inverse Laplace transformations, Application of Laplace Transforms in circuit analysis.

Module IV: Network Theorems
Reciprocity theorem, Superposition theorem, Thevenin's and Norton's theorems, Millman's theorem, Maximum power transfer theorem, Compensation theorem, Tellegan's theorem.

Module V: Two port Network & Network Functions
Introduction, two port z-, y-, T-, h-parameters, Inter-relations among parameters, Condition for reciprocity and symmetry, Interconnections of two port networks, Driving point and transfer functions, Poles, Zeros and necessary condition for driving point and transfer function,.

Module VI: Network Synthesis
Hurwitz polynomial, Positive real functions, synthesis of LC, RC, RL immittance functions.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

Text:

- M.E. Valkenburg, "Network analysis", PHI.
- D. R. Choudhary, "Networks and Systems", New Age International.
- K.M. Soni, 2009, "Circuits and Systems", VIII Edition, S.K. Kataria& Sons Delhi.

References:

- Bhise, Chadda, Kulshreshtha, "Engineering network analysis and filter design", Umesh Publication.
- F.F. Kuo, "Network Analysis and Synthesis", Wiley India Pvt. Ltd.

JAVA PROGRAMMING

Course Code: ECE2304 **CreditUnits: 03**

Course Objective:
The objective is to impart programming skills used in this object oriented language java.
The course explores all the basic concepts of core java programming. The students are expected to learn it enough so that they can develop the web solutions like creating applets etc.

Course Contents:
Module I
Concepts of OOP, Features of Java, How Java is different from C++, Data types, Control Statements, identifiers, arrays, operators. Inheritance: Multilevel hierarchy, method overriding, Abstract classes, Final classes, String Class.

Module II
Defining, Implementing, Applying Packages and Interfaces, Importing Packages. Fundamentals, Types, Uncaught Exceptions, Multiple catch Clauses, Java's Built-in Exception.

Module III
Creating, Implementing and Extending thread, thread priorities, synchronization suspending, resuming and stopping Threads, Constructors, Various Types of String Operations. Exploring Various Basic Packages of Java: Java.lang, Java. util, Java.i.o

Module IV
Event handling Mechanism, Event Model, Event Classes, Sources of Events, Event Listener Interfaces
AWT: Working with Windows, AWT Controls, Layout Managers

Module V
AppletClass, Architecture, Skeleton, Display Methods.
Swings: Japplet, Icons, labels, Text Fields, Buttons, Combo Boxes.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:
- JAVA The Complete Reference by PATRICK NAUGHTON & HERBERT SCHILD, TMH
- Introduction to JAVA Programming a Primer, E. Balaguruswamy.

References:
- "Introduction to JAVA Programming" Daniel/Young PHI
- Jeff Frentzen and Sobotka, "Java Script", Tata McGraw Hill,1999

ANALOG ELECTRONICS- I LAB

Course Code: ECE2305 **CreditUnits: 01**

Course Contents:

1. To study and plot the characteristics of a junction diode.

2. To study Zener diode I-V characteristics.

3. To study diode based clipping and clamping circuits.

4. To study half wave, full wave and bridge rectifier with filters.

5. To study the input and output characteristics of a transistor in its various configurations(CE and CB).

6. To study and plot the characteristics of a JFET in its various configurations.

7. To study and plot the characteristics of a MOSFET in its various configurations.

8. To study various types of Bias Stabilization for a transistor.

9. To study the gain and plot the frequency response of a single stage transistor amplifier.

10. To measure gain and plot the frequency response of double stage RC coupled amplifier.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

CIRCUITS & SYSTEMS LAB

Course Code: ECE2306 **CreditUnits: 01**

List of Experiments:

1. To verify Thevenin's theorem in a given network.
2. To verify reciprocity theorem in a given network.
3. To verify maximum power transfer theorem in a given network.
4. To verify Tellegen's theorem in a given network.
5. To determine the Z- and Y- parameters of a resistive two-port network.
6. To determine the T- (ABCD) parameters of a resistive two-port network.
7. To determine the h- parameters of a resistive two-port network.
8. To design series-series connection of 2 two-port networks and determine its Z- parameters.
9. To design parallel-parallel connection of 2 two-port networks and determine its Y- parameters.
10. To design a cascade connection of 2 two-port networks and determine its T- (ABCD) parameters.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

JAVA PROGRAMMING LAB

Course Code: ECE2307 **CreditUnits: 01**

Software Required: JDK1.3

Assignments will be provided for the following:

- Java programs using classes & objects and various control constructs such as loops etc, and data structures such as arrays , structures and functions
- Java programs for creating Applets for display of images and texts.
- Programs related to Interfaces & Packages.
- Input/Output and random files programs in Java.
- Java programs using Event driven concept.
- Programs related to network programming.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

SIGNALS AND SYSTEMS

Course Code: ECE2309 **CreditUnits: 03**

Course Objective:
The objective of the course is to provide knowledge of Signals and Systems to students of ECE. This Course includes good insight of types of signals and types of systems, various operations performed on them through the use of Fourier series, Fourier transform, z transform.

Course Contents:

Module I: Signals and Systems
Introduction of signals and systems; classification of signal, continuous time and discrete time signals, operations performed on them, even and odd signals, periodic and non periodic signals, deterministic and random signals, energy signals, power signals, elementary signals: impulse, step, ramp and exponentials, classification of systems.

Module II: LTI system
Response of LTI system for continuous and discrete time systems, Impulse response, Step response, properties of continuous LTI and discrete LTI systems, LTI systems described by differential and difference equation, analysis of LTI Systems, interconnection of systems.

Module III: Fourier series
Representation of continuous time periodic signal, properties of continuous time Fourier series, representation of discrete time periodic signals, convergence of the Fourier series, properties of discrete time Fourier series, Fourier series and LTI systems.

Module IV: Fourier Transform
Continuous time Fourier transform, properties of continuous time Fourier transform, discrete time Fourier transform, properties of discrete time Fourier transform; applications; Bandwidth determination of signals and systems.

Module V: z-Transform
Definition of z-transform, region of convergence, properties of z-transform, first order system, second order system, inverse z-transform, analysis of LTI system using z-transform.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References

Text:

- Alan.V Oppenheim, Signals and Systems, 4th Edition 2007, Pearson Prentice Hall Publication.
- K.M. Soni, Signals and Systems; 3rd Edition, S.K. Kataria& Sons Publication.
- P.RameshBabu, Signal and Systems, 3rd Edition, Scitech Publications (INDIA) Pvt. Ltd.

References:

- Simon Haykin, Signals and Systems, 2nd Edition, Willy Publications.
- B.P.Lathi, Linear Systems & Signals, 2nd Edition, Oxford Publication.
- Roberts, Fundamentals of Signals and Systems, TMH Publication.

DATA STRUCTURES USING C

Course Code: ECE2311 **CreditUnits: 02**

Course Objective:
Data structure deals with organizing large amount of data in order to reduce space complexity and time requirement. This course gives knowledge of algorithms, different types of data structures and the estimation space and time complexity.

Course Contents:
Module I: Introduction to Data structures
Data structures: Definition, Types. Algorithm design, Complexity, Time-Space Trade offs. Use of pointers in data structures.
Array Definition and Analysis, Representation of Linear Arrays in Memory, Traversing of Linear Arrays, Insertion And Deletion, Single Dimensional Arrays, Two Dimensional Arrays, Multidimensional Arrays, Function Associated with Arrays, Character String in C, Character String Operations, Arrays as parameters, Implementing One Dimensional Array, Sparse matrix.

Module II: Introduction to Stacks and queue
Stack: Definition, Array representation of stacks, Operations Associated with Stacks- Push & Pop, Polish expressions, Conversion of infix to postfix, infix to prefix (and vice versa),Application of stacks recursion, polish expression and their compilation, conversion of infix expression to prefix and postfix expression, Tower of Hanoi problem.
Queue: Definition, Representation of Queues, Operations of queues- QInsert, QDelete, Priority Queues, Circular Queue, Deque.

Module III: Dynamic Data Structure
Linked list: Introduction to Singly linked lists: Representation of linked lists in memory, Traversing, Searching, Insertion into, Deletion from linked list, doubly linked list, circular linked list, generalized list. Applications of Linked List-Polynomial representation using linked list and basic operation.
Stack and queue implementation using linked list.

Module IV: Trees and Graphs
Trees: Basic Terminology, Binary Trees and their representation, expression evaluation, Complete Binary trees, extended binary trees, Traversing binary trees, Searching, Insertion and Deletion in binary search trees, General trees, AVL trees, Threaded trees, B trees.
Graphs: Terminology and Representations, Graphs & Multigraphs, Directed Graphs, Sequential representation of graphs, Adjacency matrices, Transversal Connected Component and Spanning trees.

Module V: Sorting and Searching and file structures
Sorting: Insertion Sort, Bubble sort, Selection sort, Quick sort, two-way Merge sort, Heap sort, Partition exchange sort, Shell sort, Sorting on different keys, External sorting.
Searching: Linear search, Binary search

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:

- Horowitz and Sahani, "Fundamentals of Data structures", Galgotia publications
- Tannenbaum, "Data Structures", PHI
- R.L. Kruse, B.P. Leary, C.L. Tondo, "Data structure and program design in C" PHI
- "Data structures and algorithms" – Schaum Series.

DATA STRUCTURES USING C LAB

Course Code: ECE2312 **CreditUnits: 01**

Software Required: Turbo C++

Assignment will be provided for following:

- Practical application of sorting and searching algorithm.
- Practical application of various data structure like linked list, queue, stack, tree

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

VIRTUAL INSTRUMENTATION

Course Code: ECE2313 **CreditUnits: 02**

Course objective: The purpose of this course is to provide a thorough introduction to virtualinstrumentation with an in depth study of virtual instrument, software, hardware and its applications.

Course Contents:

Module I:Introduction to Virtual Instrumentation:
Introductions, Historical perspective, advantages, block diagram and architecture of a virtual instrument, conventional vs. virtual instrumentation.

Module II:Introduction to Software :
Introduction to Lab VIEW, Front panel, back panel representations, Block diagram, Menus, Palettes, VI and Sub VI, Editing and Debugging VI, Structures, Arrays, Clusters, Charts and Graphs, Data acquisition, Instrument Control, Signal Generation and Signal Processing Examples.

Module III: Introduction to systems hardware:
ADC, DAC, D/O, counters and timer, PC hardware structure, timing, interrupts, DMA, software and hardware installation, Configuring data acquisition hardware using the drives in application software, use of DAQ library functions for different analog and digital input/output operations. Input/output devices & functions like data gloves, joysticks, CRT etc.

Module IV:Application of Virtual Instrumentation in various fields:
Aviation, Automotive, High Voltage, Defense, Chemical, Industrial, Marine, Medical, Mining, Nuclear Energy, Virtual landscapes.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

LABORATORY / FIELD EXPERIENCES

- **.** Geographical programming using Lab VIEW
- . Applications of Lab VIEW

Text & references:

- . Learning with LabVIEW 7 Express – R.H. Bishop, Pearson Education, Delhi.
- . LabVIEW Basic 1 Course Manual, National Instruments
- Virtual Instrumentation Using LabVIEW- Sanjay Gupta & Joseph John, TMG; 2005.
- LabVIEW for everyone -Wells Lisa K and Travis Jeffrey, Prentice Hall.

VIRTUAL INSTRUMENTATION LAB

Course Code: ECE2314 **CreditUnits: 01**

List of Experiments:

1. To open, and explore the components of LabView.
2. To build a simple VI that converts a Celsius temperature reading to Fahrenheit.
3. (a) To create an icon and a connector pane so you can use a VI as a subVI.
   (b) To build a VI and create its icon and connector pane so you can use it as a subVI.
4. To build a VI to generate 4*5 two dimensional array of random numbers (between1 to 2).
5. To Build a VI that generate Fibonacci series starting from '0'.
6. To build a VI which finds roots of quadratic equation using formula node.
7. To build a VI that reverses the contents of an array.
8. To build a VI that can be used for sorting of numeric array i.e. in ascending or descending order.
9. To build a VI for 4*1 multiplexer operation.
10. To build a VI for 3*8 Decoder operation.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

Syllabus - Fourth Semester

COMMUNICATION SYSTEMS

Course Code: ECE2402 **CreditUnits: 03**

Course Objective:
The purpose of this course is to provide a thorough introduction to analog and digital communications with an in depth study of various modulation techniques, Random processes are discussed, and information theory is introduced.

Course Contents:

Module I: Introduction
Communication Process, Source of Information, base-band and pass-band signals, Review of Fourier transforms, Random variables, different types of PDF, need of modulation process, analog versus digital communications

Module II: Amplitude Modulation
Amplitude modulation with full carrier, suppressed carrier systems, single side band transmission, switching modulators, synchronous detection, envelope detection, effect of frequency and phase errors in synchronous detection, comparison of various AM systems, vestigial side band transmission.

Module III: Angle Modulation
Narrow and wide band FM, BW calculations using Carson rule, Direct & Indirect FM generations, phase modulation, Demodulation of FM signals, noise reduction using pre & de-emphasis.

Module IV: Pulse Modulation
Pulse amplitude, width & position modulation, generation & detection of PAM, PWM & PPM, Comparison of frequency division and time division multiplexed systems.
Basics of Digital Communications: ASK, PSK, FSK, QPSK basics & waveform with brief mathematical introduction

Module V: Noise
Different types of noise, noise calculations, equivalent noise band width, noise figures, effective noise temperature, noise figure.

Module VI: Introduction to Information Theory
Measurement of Information, mutual, Shannon's theorem, Source coding, channel coding and channel capacity theorem, Huffman code

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

- B. P. Lathi: "Modern analog& digital communication", OXFORD Publications
- Wayne Tomasi: "Electronic Communication systems", Pearson Education, 5th edition
- Simon Haykin, "Communication Systems", John Wiley & Sons, 1999, Third Edition.
- Taub and schilling, "Principles of Communication Systems" TMH

ANALOG ELECTRONICS-II

Course Code: ECE2403 **CreditUnits: 03**

Course Objective:
The purpose of this course is to introduce the student to the application of semiconductor devices in linear analog circuits. To insure the usefulness of the course material to both computer engineers and electrical engineers, the course stresses circuit designs using the operational amplifier.

Course Contents:

Module I: Building Blocks of Analog ICs
Differential amplifier, Op-amp Model, op-amp DC & AC parameters, virtual ground, Current mirrors, Active loads, Level shifters and output stages.

Module II: Operational amplifiers
Introduction, open loop and closed loop configuration, op-amp parameters (input offset current, output offset current, i/p bias current, CMRR, PSRR, null adjustment range, etc,) Inverting and non-inverting configuration, voltage gain of inverting and non inverting configurations.

Module III: Linear & Non Linear Wave shaping
Adders, Voltage to current, current to voltage Converter, Integrators, Differentiators**,** Voltage follower (voltage buffer), summer, subtractor, Comparators, log/antilog circuits using Op-amps, precision rectifiers

Module IV: Waveform Generations
Damped and undamped oscillations, Barkhausen criterion for sustained oscillation.Tank circuit generator Astable multi Vibrators, OTA-C Oscillators, Crystal oscillator**.**Types of oscillators: LC-Hartley and Colpitts, RC-RC phase shift and Wien bridge oscillator, Basics of tuned Amplifiers, Voltage Controlled Oscillator.

Module V: Active RC Filters & Applications of Linear Circuits
Idealistic & Realistic response of filters (LP, BP, and HP), Butter worth & Chebyshev approximation filter functions, LP,BP,HP and All pass, Notch Filter, Operational transconductance amplifier (OTA)-C filters.

Module VI: Applications of IC Analog Multiplier & Timer
IC phase locked loops, 555 Timer, IC voltage regulators-(fixed, variable) 78xx, 79xx series and adjustable.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

- Richard C. Jaeger: Microelectronic Circuit Design
- Adel S. Sedra and K. C. Smith: Microelectronic Circuits
- RamakantGaekwad: Operational Amplifiers
- Rolf Schaumann and Mac E. Van Valkenburg: Design of Analog Filters
- D. Roy Choudhury and Shail B. Jain: Linear Integrated Circuits

ELECTROMAGNETIC FIELD THEORY

Course Code: ECE2404 **CreditUnits: 03**

Course Objective:
This course provides a general introduction to the important physical concepts and mathematical methods used in treating all types of wave phenomena, but stresses electromagnetic signal propagation and issues of central importance in electrical engineering. As a core course in the Electrical Computer and Systems Engineering option of the Engineering Sciences concentration, it provides essential background and basic preparation for more advanced work in device physics, microwave and ultra-fast circuitry, antenna design, optics, optical communication and optoelectronics.

Course Contents:

Module I: Mathematical Basics and Electrostatics
Coordinate Systems: Spherical and Cylindrical coordinates, Dirac delta function, Coulomb's law, Gauss's law, Poisson's Equation, Laplace's Equation, Electrostatic Boundary conditions, Work and Energy in Electrostatics, Conductors, Surface charge and force on conductors

Module II: Magnetostatics and Magnetic Fields in matter
Magnetic induction and Faraday's law, Magnetic Flux density, Magnetic Field Intensity, BiotSavart Law, steady currents, Ampere's law, Magnetostatic Boundary conditions, magnetic field inside matter, magnetic susceptibility and permeability, ferromagnetism, energy stored in a Magnetic field, Magnetic Vector Potential

Module III: Electrodynamics
Faraday's laws, Maxwell's equations, Maxwell's modification of Ampere's law, continuity equation and Poynting theorem.

Module IV: Electrodynamic Waves
Wave propagation in unbounded media, Boundary conditions, reflection and transmission, polarization, E.M. waves in vacuum, E. M. waves in matter: reflection and transmission of plane waves.

Module V: Introduction to Transmission Lines
Transmission Line, Line Parameters, Characteristic Impedance, Image Impedance, HVDC and HVAC Common faults in transmission lines.Skin Effect, Ferranti Effect and Corona.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

- Griffiths: Introduction to Electrodynamics
- Fawwaz T. Ulaby:Fundamentals of Applied Electromagnetics
- Hayt, William H., Buck, John A. Hayt, William H., Buck, John A., Engineering Electromagnetics

DIGITAL ELECTRONICS

Course Code: ECE2411 **CreditUnits: 02**

Course Objective:
This course is an introduction to the basic principles of digital electronics. At the conclusion of this course, the student will be able to quantitatively identify the fundamentals of computers, including number systems, logic gates, logic and arithmetic subsystems, and integrated circuits. They will gain the practical skills necessary to work with digital circuits through problem solving and hands on laboratory experience with logic gates, encoders, flip-flops, counters, shift registers, adders, etc. The student will be able to analyze and design simple logic circuits using tools such as Boolean Algebra and Karnaugh Mapping, and will be able to draw logic diagrams.

Course Contents:

Module I: Boolean Functions
Analog & digital signals, AND, OR, NOT, NAND, NOR , XOR & XNOR gates, Boolean algebra, DeMorgan's theorems, Implementation of logical function using only NAND/NOR gates, 1`s complement and 2`s complement, BCD to Gray and Gray to BCD code conversion, Standard representation of logical functions (SOP and POS forms), K-map representation and simplification of logical function up to five variables, don't care conditions, XOR & XNOR simplifications of K-maps, Tabulation method.

Module II: Combinational Circuits
Adders, Subtractors, Implementation of full adder using half adder, full subtractor using half subtractor, Multiplexer, de-multiplexer, decoder & encoder, code converters, 1 & 2 bit comparators, BCD to seven segment decoder/encoder, Implementation of logic functions using multiplexer/de-multiplexer and decoder, Implementation of 16×1 MUX using 4×1 MUX, 4×16 decoder using 3×8 decoder etc., logic implementations using PROM, PLA & PAL.

Module III: Sequential Circuits
Difference between combinational and sequential circuits, Latch, Flip-flops: SR, JK, D & T flip flops – Truth table, Excitation table, Conversion of flip-flops, set up and hold time, race around condition, Master Slave flip flop, Shift registers: SIPO, PISO, PIPO, SIPO, Bi-directional, 4-bit universal shift register; Counters: Asynchronous/ripple & synchronous counters – up/down, Ring counter, sequence detector.

Module IV: Logic families & data converters
Logic families: Special characteristics (Fan out, Power dissipation, propagation delay, noise margin), working of RTL, DTL, TTL, ECL and CMOS families; Data converters: Special characteristics, ADC – successive approximation, linear ramp, dual slope; DAC – Binary Weighted, R-2R ladder type.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

- MorisMano : Digital Design, Pearson Education.
- R. P. Jain: Digital Electronics, Tata McGraw Hill.
- Thomas L. Floyd: Digital Fundamentals, Pearson Education.
- Malvino and Leech: Digital Principles & Applications, Tata McGraw Hill.

COMMUNICATION SYSTEMS LAB

Course Code: ECE2406 **CreditUnits: 01**

List of Experiments:

1. To study the sampling and reconstruction of a given signal.

2. To study amplitude modulation and demodulation.

3. To study frequency modulation and demodulation.

4. To study time division multiplexing.

5. To study pulse amplitude modulation.

6. To study delta and adaptive delta modulation and demodulation.

7. To study carrier modulation techniques using amplitude shift keying and Frequency shift keying.

8. To study carrier modulation techniques using binary phase shift keying and differential shift keying.

9. To study pulse code modulation & differential pulse code modulation as well as relevant demodulations.

10. To study quadrature phase shift keying & quadrature amplitude modulation.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

ANALOG ELECTRONICS–II LAB

Course Code: ECE2407 **CreditUnits: 01**

List of Experiments:

1. To study the op amp as an inverting and non inverting amplifier.

2. To use the op amp as an adder, subtractor, integrator and differentiator.

3. To design a ramp and a square wave generator.

4. To study the IC-555 timer as stable and bistablemultivibrator.

5. To design low pass, high pass and band pass filters using op- amp. and plot their frequency response.

6. To design and study class a power amplifier.

7. To design and study a class B push pull amplifier.

8. To study various feedbacks such as voltage series feedback.

9. To design RC phase shift and Wein bridge oscillators using op amplifier.

10. To design and study Colpitt and Hartley oscillators.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

DIGITAL ELECTRONICS LAB

Course Code: ECE2412 **CreditUnits: 01**

List of Experiments:

1. To verify the truth tables of NOT, OR, AND, NOR, NAND, XOR, XNOR gates.
2. To obtain half adder, full adder using gates and verify their truth tables.
3. To obtain half subtractor, full subtractor using gates and verify their truth tables.
4. To implement control circuit using multiplexer.
5. To convert BCD code into excess 3 code and verify the truth table.
6. To verify the truth tables of RS, D, JK and T flip- flops.
7. To implement and verify 3-bit bi-directional shift register.
8. To design and study asynchronous/ripple counter.
9. To design and study synchronous counter.
10. To design and study a sequence detector.

Examination Scheme:

IA				**EE**	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

ORCAD LAB

Course Code: ECE2413 **CreditUnits: 01**

Course Contents:

1. To simulate and obtain PCB layout for a 2 bit x 2 bit combinational multiplier
a) Using 4 to 1 line multiplexer and logic gates.
b) Using 1:16 demultiplexer.

2. To simulate and obtain PCB layout for : BCD to EXCESS 3 codes converter using
a) 8:1 multiplexer.
b) 4:1 multiplexer and gates.

3. To simulate and obtain PCB layout for BCD to seven segment decoder using gates.

4. To simulate and obtain PCB layout for BCD to Gray Code using
a) 8:1 MUX
b) Decoder
c) 4:1 MUX

5. To simulate and obtain PCB layout for a Gray Code to BCD converter using
    a) 4:1 MUX
    b) 1:16 DEMUX

6. To simulate and obtain PCB layout for BCD to EXCESS 3 converter using minimum number of NAND gates.

7. To simulate and obtain PCB layout for digital clock a circuit which display
Hours, minutes and seconds using CPLD/FPGA.

8. To design, simulate and make a PCB layout of a circuit for traffic signal control having road at a junction using
a) MUX
    b) Counters
c) CPLD/FPGA

9. To design, simulate and make a PCB layout of a square wave generator using 7414 IC.

10. To design, simulate and make a PCB layout for two bit RAM using 7400, 7403 gates.

11. To design, simulate and make a PCB layout for 64 bit RAM using 7489 IC.

12. To design, simulate and make a PCB layout for voltage multiplier circuit using operational amplifier with (IC type 741CC/Fairchild 741DC/Motorola MC 1741 CL/Signetics NT 741 A/National LM741 CD, LM741 CN-14/Taxas Instruments SN 72741 N, SN 2741 J)

13. To design, simulate and make a PCB layout for D/A conversion – decade BCD.

To design and simulate:

14. a) 2 bit x 2 bit combinational multiplier using 1:16 demultiplexer.

15. a) BCD to seven segment decoder using gates.

16. BCD to Gray code converter using
a) 8:1 MUX
b) Decoder

17. Gray code to BCD converter using 1:16 demultiplexer.

18. BCD to excess code converter using minimum number of gates.
19. 64 bit RAM using 16x4 RAM (IC 7489).
20. Inverting and non inverting amplifier with gain more than 100 using op amp (UA 741 IC).
21. Integrator and differentiator using IC UA 741.
22. Full wave rectifier.
23. Transistor as an amplifier.
24. Diode and transistor realization of AND, OR & NOT gates.

Examination Scheme:

IA				**EE**	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

PCB FABRICATIONS

Course Code: ECE2414 **CreditUnits: 02**

Course Objective:
To equip the students with the knowledge of PCB design and fabrication processes.
Objective:

- To make familiar with PCB design and various processes involved.
- To provide in-depth core knowledge in design, performance analysis and fabrication of Printed Circuit Boards.
- To provide the knowledge in PCB fabrication process and factors affecting PCB performance.

Course Contents:

Module I: Introduction to the PCB

Definition and Evolution of the Printed Circuit Board (PCB), Purposes of a PCB, Applications, Market Drivers, Typical Development Flow for a PCB, Printed Circuit Technology, Basic Electronic Components, Resistors, Capacitors, Inductors, Diodes, Transistors, Relays, Connectors, Integrated Circuits: How a silicon wafer becomes an IC, Printed Circuit Board Characteristics, PCB Materials, Fillers, resins, laminates, base material characteristics, Dielectric, conductors, Engineering References

Module II: Design and Analyses

Design and Environmental Requirements: Functional, Thermal, Vibration, Shock, EMI/EMC; Electrical Engineering: Analog and digital signals, Signal integrity, Grounding concepts, Current carrying capacity, CAD, Schematics, Layout rules of thumb; Mechanical Engineering: Panels, Standard board sizes, Packaging, Thermal Design, Heat transfer basics, Convection, Conduction, PCB Thermal Design Features, Thermal modeling, Cycling and fatigue , Component Vibration Fatigue, Vibration Models and Terminology, Combined Thermal and Structural Fatigue

Module III: Contamination Control/Environmental Control

Contamination Control, Conformal Coatings, Polluting Agents, Safety Controls, Pollution Controls, Recycling, Standards; Manufacturing: PCB Manufacturing Information, PCB Layout and Artwork; Fabrication: Machining Operations, Blanking, Cutting, Punching, Drilling, Laminating Techniques, Plating, Etching, Surface Finishing, Conformal Coatings, Inspection and Checkout, Specifications and Standards.

Module IV: Assembly

PCB Assembly Drawing Examples, Component Considerations, Component mounting and support , Mechanical Devices, Soldering Technology, Nonsolder Connections, Cleaning, Parts Staking, Conformal Coating Removal, Repair and Rework, Safety Considerations, ESD protection, Specifications and Standards.

Module V: Testing & Quality Assurance

Common PCB Production Faults, Bare Board Testing, Electrical Performance Testing, Assembled PCB Testing, Quality Assurance in Design, FMEA – Failure Mode and Effects Analysis, Software Tools, Quality Assurance in Manufacturing and in Assembly, Specifications and Standards.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

- Jon Uarteresian, 2002, “Fabricating Printed Circuit Boards”, Newnes (Elsevier Science)
- RS Khandpur, 2008, “Printed Circuit Boards”, Tata McGraw-Hill Education
- Christopher T Robertson, 2004, “Printed Circuit Board: Designer's Reference, Basics”, Prentice Hall Professional, 2004
- Charles Harper, 2000, “High Performance Printed Circuit Boards”, McGraw-Hill Education

DATABASE MANAGEMENT SYSTEMS

Course Code: ECE2415 **CreditUnits: 02**

Course Objective:
The objective of this course is to get students familiar with Databases and their use. They can identify different types of available database model, concurrency techniques and new applications of the DBMS.

Course Contents:
Module I: Introduction
Concept and goals of DBMS, Database Languages, Database Users, Database Abstraction.
Basic Concepts of ER Model, Relationship sets, Keys, Mapping, Design of ER Model

Module II: Hierarchical model &Network Model
Concepts, Data definition, Data manipulation and implementation.Network Data Model,

Module III: Relational Model
Relational database, Relational Algebra, Relational & Tuple Calculus.

Module IV: Relational Database Design and Query Language
SQL, QUEL, QBE, Normalization using Functional Dependency, Multivalued dependency and Join dependency.

Module V: Concurrency Control and New Applications
Transaction basics: ACID property, Lifecycle of Transcation, Why Concurrency Control, Schedule, Lock Based Protocols, Time Stamped Based Protocols, Multi version locking,Deadlock Handling, Recovery schemes using immediate and deferred update

Module V1 Distributed Database
Distributed Database, Fragmentation and Replication in distributed database, Distributed database architecture. Object Oriented Database, Multimedia Database

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:
- Korth, Silberschatz, "Database System Concepts", 4th Ed., TMH, 2000.
- Steve Bobrowski, "Oracle & Architecture", TMH, 2000

References:
- Date C. J., "An Introduction to Database Systems", 7th Ed., Narosa Publishing, 2004
- Elmsari and Navathe, "Fundamentals of Database Systems", 4th Ed., A. Wesley, 2004
- Ullman J. D., "Principles of Database Systems", 2nd Ed., Galgotia Publications, 1999.

DATABASE MANAGEMENT SYSTEMS LAB

Course Code: ECE2416 **CreditUnits: 01**

Software Required: Oracle 9i /10i/11i/MySQL/PostgreSQL
Topics covered in lab will include:

- Database Design
- Data Definition (SQL)
- Data Retrieval (SQL)
- Data Modification (SQL)
- Views
- Triggers and Procedures
- PL\SQL

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

Syllabus - Fifth Semester

DIGITAL CIRCUITS AND SYSTEMS

Course Code: ECE2501 **CreditUnits: 03**

Course Objective:
This course builds on the course Digital Circuits and Systems - Hardware development language VHDL is introduced; the usage of the same to implement the systems is dealt in detail.

Course Contents:

Module I: Design of Sequential circuits
SR, JK, T and D flip flops and their timing diagrams with delay, characteristic table, characteristic equation and excitation tables. Design of Finite State Machines: Mealy and Moore type using next state tables, state diagrams, state minimization, state encoding: minimum bit change and hot one encodings. Comparative cost and delays of different implementations and their optimization and timing diagrams, Asynchronous and synchronous sequential circuits Static Timing Analysis –setup, hold time, clock skew, clock period
Data paths, FSMs with datapaths, ASM charts

Module II: Basics of VHDL
Introduction and Basic Design Units of VHDL, Writing Entities for Digital circuits like decoders, registers etc, Scalar Data types and Operations: Object types: constants, variables, signal and files. Data Types: scalar, integer, floating, physical, enumeration, type declarations, subtypes, expressions and operators for various types.
Sequential statements: If, case, Null, Loop, Exit, Next statements, while loops, For loops, Assertion and report statements
Composite Arrays: arrays, Array aggregates, unconstrained array types, strings, Bit vectors, Standard Logic Arrays, array operations and records

Module III: VHDL Programming
Behavioral Modeling: process statements, variable and signal assignments, inertial and transport delay models, signal drivers, multiple and postponed processes
Dataflow Modeling: Concurrent signal assignment, multiple drivers, block statement
Structural Modeling: component declaration, component instantiation, resolving signal values, and configuration: basic configuration, configuration for structural modeling, mapping library entities.
Generics, generic (AND, NAND, OR, NOR, XOR and XNOR) gates, functions and subprograms, packages and libraries

Module IV: Synthesis: mapping statements to gates
Writing a test bench, converting real and integers to time, dumping and reading from text file
Vhdl modeling of basic gates, half and full adder AOI, IOA, OAI, multiplexes, decoders (dataflow, behavioral and structural modeling), three state driver, parity checker, D, T, JK and SR flip flops, flip flops with preset and clear, modeling for multiplexer, priority encoder, ALU etc, modeling regular structures, delays, conditional operations, synchronous logic, state machine modeling, Moore and Mealy machines, generic priority encoder, clock divider, shift registers, pulse counter etc

Module V: Overview of the following
PLD devices, PROM, PAL, PLA, CPLD, EPLD GAL, FPGA, DRAM etc and their applications, FPGA programming, Design exercises ASIC design using CAD tools

Examination Scheme:

Components	HA	V/S/Q	CT	AT	ESE
Weightage (%)	7	8	10	5	70

Text & References:

- Daniel Gajski: Principles of Digital Design
- Bhasker: A VHDL Primer 3/e
- Pedroni: Circuit Design with VHDL
- Perry: VHDL: Programming by examples K. Skahill, VHDL for programmable Logic

DIGITAL COMMUNICATIONS

Course Code: ECE2502 **CreditUnits: 02**

Course Objective:
The purpose of this course is to provide a thorough introduction to digital communications with an in depth study of various modulation techniques, receiver design & performance analysis are discussed.

Course Contents:

Module I:Digital Communication System Basics
Basic building blocks of Digital communications, analog versus digital communication, Advantages disadvantages of digital communications.

Module II: Digital Baseband Transmission
Pulse code modulation, Signal to quantization ratio, non-uniform quantization companding, BW calculations.

Module III: Transmission of Analog Samples & Signal Detection in Noise
Delta Modulation, Adaptive delta-modulation, DPCM, ADCM, ADPCM, Matched Filter Receiver, Derivation of Its Impulse Response and Peak Pulse Signal to Noise Ratio. Correlator receiver, Decision Threshold and Error Probability For, Unipolar (ON-OFF) Signaling, ISI, Nyquist Criterion For Zero ISI & Raised Cosine Spectrum

Module IV: Digital Modulation Technique.
Gram-Schmidt Orthogonalization Procedure, Types of Digital Modulation, Wave forms for Amplitude, Frequency and Phase Shift Keying, Method of Generation and Detection of Coherent & Non-Coherent Binary ASK, FSK & PSK Differential Phase Shift Keying, Quadrature Modulation Techniques QPSK, Probability of Error and Comparison of Various Digital Modulation Techniques.

Module V: Digital Multiplexing
Fundamentals of Time Division Multiplexing, Electronic Commutator, Bit, Byte Interleaving T1 Carrier System, Synchronization and Signaling of T1, TDM, PCM Hierarchy, T1 to T4 PCM TDM System (DS1 to DS4 Signals)

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

- Simon Haykin: "Digital Communication", John Wiley / 4th Ed.
- Bernard SKLAR: "Digital communication", Pearson education.
- Lathi, B.P / "Modern Digital & Analog Communication Systems" / Oxford University Press /.
- Prokis J.J / "Digital Communications" / McGraw Hill /
- Wayne Tomasi: "Electronic Communication systems", Pearson Education,5th edition

CONTROL SYSTEMS

Course Code: ECE2503 **CreditUnits: 03**

Course Objective:
The basic objective of this course is to provide the students the core knowledge of control systems, in which time & frequency domain analysis, concept of stability.

Course Contents:

Module I: Input / Output Relationship
Introduction of open loop and closed loop control systems, mathematical modeling and representation of physical systems (Electrical Mechanical and Thermal), derivation of transfer function for different types of systems, block diagram & signal flow graph, Reduction Technique, Mason's Gain Formula.

Module II: Time – Domain Analysis
Time domain performance criteria, transient response of first, second & higher order systems, steady state errors and static error constants in unity feedback control systems, error criteria, generalized error constants, performance indices, response with P, PI and PID Controllers.

Module III: Frequency Domain Analysis
Polar and inverse polar plots, frequency domain specifications, Logarithmic plots (Bode Plots),gain and phase margins, relative stability, Correlation with time domain, constant close loop frequency responses, from open loop response, Nyquist Plot.

Module IV: Concept of Stability
Asymptotic stability and conditional stability, Routh – Hurwitz criterion, Root Locus plots and their applications. Compensation Techniques:Concept of compensation, Lag, Lead and Lag-Lead networks, design of closed loop systems using compensation techniques. P, PI, PID controllers.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:
- Dr. N.K Jain, 2005,"Automatic Control System Engineering", Dhanpat Rai Publication.
- J. Nagrath& M. Gopal, 2000, "Control System Engineering", New Age International.

References:
- M, K. Ogata, 2002, "Modern Control Engineering, PHI.
- B. C. Kuo, 2001, "Automatic Control system, Prentice Hall of India.

MICROPROCESSOR SYSTEMS

Course Code: ECE2509 **CreditUnits: 03**

Course Objective:
This course deals with the systematic study of the Architecture and programming issues of 8085-microprocessor family. The aim of this course is to give the students basic knowledge of the above microprocessor needed to develop the systems using it.

Course Contents:

Module I: Introduction to Microcomputer Systems
Introduction to Microprocessors and microcomputers, Study of 8 bit Microprocessor, 8085 pin configuration, Internal Architecture and operations,interrupts, Stacks and subroutines, various data transfer schemes.

Module II: ALP and timing diagrams
Introduction to 8085 instruction set, advance 8085 programming , Addressing modes, Counters and time Delays, Instruction cycle, machine cycle, T-states, timing diagram for 8085 instruction.

Module III: Memory System Design & I/O Interfacing
Memory interfacing with 8085. Interfacing with input/output devices (memory mapped, peripheral I/O), Cache memory system. Study of following peripheral devices 8255, 8253, 8257, 8259, 8251.
Module IV: Architecture of 16-Bit Microprocessor
Difference between 8085 and 8086, Block diagram and architecture of 8086 family, pin configuration of 8086, minimum mode & maximum mode Operation, Bus Interface Unit, Register Organization, Instruction Pointer, Stack & Stack pointer, merits of memory segmentation, Execution Unit, Register Organization.

Module V: Pentium Processors
Internal architecture of 8087, Operational overview of 8087, Introduction to 80186, 80286, 80386 & 80486 processors, Pentium processor (P-II, P-III, P-IV).

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

- Ramesh. S. Gaonkar, "Microprocessor architecture Programming and Application with 8085" Penram International Publishing, 4th Edition
- B. Ram, "Fundamentals of microprocessors and microcomputer" Dhanpat Rai, 5th Edition.]
- Douglas V Hall.
- M. Rafiquzzaman, "Microprocessor Theory and Application" PHI – 10th Indian Reprint.
- Naresh Grover, "Microprocessor comprehensive studies Architecture, Programming and Interfacing" Dhanpat Rai, 2003.
- Gosh," 0000 to 8085" PHI.

DIGITAL CIRCUITS AND SYSTEMS LAB

Course Code: ECE2504 **CreditUnits: 01**

List of Experiments

To implement VHDL code for

1. 2, 3, 4 inputs AND, OR, XOR and XNOR gates and testing their simulation with signals.
2. Half adder, full adder and full subtractor. Also trying out other simple combinatorial circuits like AOI, IOA, OAI.
3. D and T, flip-flops.
4. JK and SR flip-flops.
5. 2 to 4 and 3 to 8 decoders.
6. 2 to 1, 4 to 1 and 8 to 1 multiplexers.
7. a register.
8. 2 to 1, 4 to 2 and 8 to 3 priority encoders.
9. 8 bit tri state drivers.
10. 9 input parity checker.
11. 1 bit, 4 bit 8 bit comparators.
12. Adding and subtracting 8 bit integers of various types.
13. Clock divider
14. shift register
15. Pulse counters.
16. VHDL Design examples of Moore machine, Mealy machine, generic gate inputs and delays.
17. VHDL code examples of structural modeling showing binding.

Experiments based Field Programmable Gate Array (FPGA) Programming

18. Implementation of all the above VHDL experiments using FPGA.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

MICROPROCESSOR SYSTEMS LAB

Course Code: ECE2505 **CreditUnits: 01**

List of experiments:

1) Write at least three different programs for addition of two 8 bit numbers assuming carry may or may not be generated.

2) Write at least three different programs for subtraction of two 8 bit numbers assuming borrow may or may not be generated.

3) Write two different programs for 16 bit addition, one using instruction DAD and another without using instruction DAD.

4) Write assembly language program for 8 bit multiplication and division.

5) To study, understand, interface and two peripheral devices with 8085.

6) Any three programs using 8085 based on block of data.

7) Using 8086 write an ALP to add list of 10 given numbers.

8) Using 8086 write an ALP to sum the numbers from 1-100.

9) Using 8086 write an ALP to count negative numbers from a given list of 10 numbers.

10) Using 8086 write an ALP to check number of vowels in a given string.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva

CONTROL SYSTEMS LAB

Course Code: ECE2506 **CreditUnits: 01**

Course Contents:

1. Study and draw
a) Step response of open Loop system (linear 1st order, 2nd order
b) Step response of closed loop systems (1st order)
2. Study and draw temperature control system the open loop response and closed loop response with different values of gains
3. Study of operations and characteristics of a stepper motor
4. To Study a D.C. motor speed control system.
5. Performance evaluation and design of PID controller.
6. Study of microprocessor control of a simulated linear system.
7. To design a suitable cascade compensator for the given system and verify the resulting improvement.
8. Note: three experiments in MATLAB have to be performed in the slot of MATLAB.
Using MATLAB obtain the unit-step response and unit impulse response of the following system:

$$\frac{C(s)}{R(s)} = \frac{16}{s^2 + 1.6s + 16}$$

9. For a 2nd order transfer function using MATLAB
a) Bode Plot
b)Root locus plot
c)Nyquist plot.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva

SUMMER INTERNSHIP EVALUATION-I

Course Code: ECE2535 **CreditUnits: 03**

Methodology:

Practical training is based on the theoretical subjects studied by students. It can be arranged within the college or in any related industrial unit. The students are to learn various industrial, technical and administrative processes followed in the industry. In case of on-campus training the students will be given specific task of fabrication/assembly/testing/analysis. On completion of the practical training the students are to present a report covering various aspects learnt by them and give a presentation on same.

Examination Scheme:

Feedback from industry/work place	20
Training Report	40
Viva	15
Presentation	25
Total	**100**

BIOMEDICAL INSTRUMENTATION

Course Code: ECE2551 **CreditUnits: 03**

Course Objective:
The purpose of this course is to provide a thorough introduction to biological applications of electronic instruments with an in depth study of various instruments like ECT, EEG, EMG, X-Ray, MRI etc.

Course Content:
Module I:Sensors and Transducers for biological applications
Types, properties, characteristics and selection of transducers for biological instrumentation.

Module II:Measurement of electrical parameters
Leads and electrodes, electrocardiography, electrical activity of the heart, equivalent cardiac generator. Einthoven lead system, standardization of recording and display of ECT (Electrocardiogram), EEG (Electroencephalogram), EMG (Electromyogram), EOG (Electrooccu1ogram), ERG (Electroretinogram), EGG (Electrogastogram).

Module III:Measurement of non-electrical parameters
Blood flow, drop recorder, electromagnetic flow meter, measurement of systolic and diastolic pressures, blood pressure instruments, intraocular pressure, lung air pressure, Audiometers. Measurement of body temperature, thermography. Cardiac tachometer, respiration rate phonocardiogram, heart sounds electrical stethoscope pulmonary function analysers. CO2 - O2 - Concentration in exhaled air, blood and lungs, pH value of blood, impedance pletnysmography blood gas analysers, blood cell counters.

Module IV:Medical Imaging Systems
Medical display systems, medical thermography X-Ray, diathermy equipment. Ultrasonics in biomedical application for diagnostic and therapeutic, CAT, MRI, Laser applications in biomedical field.

Module V:Patient safety
Electrical Safety of Medical Equipments, Shock Hazards from Electrical Equipment, Methods of Accident Prevention, Test Instruments for checking Safety parameters of biomedical equipments.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

- Biomedical Instrumentation and Measurements; L.C. Cronwell F.J. Weibell. E.A. Pfeiffer, PHI.
- Principles of applied instrumentation: Gaddes and Baker, John Wiley & Sons.
- Handbook of Bio-medical Instrumentation; R.S. Khandpur, Mc Graw Hill
- Medical Instrumentation – Application & Design, John G. Webster, Editor, JohnWiley& Sons.

OPERATING SYSTEMS

Course Code: ECE2507 **CreditUnits: 03**

Course Objective:
Operating Systems serve as one of the most important courses for undergraduate students, since it provides the students with a new sight to envision every computerized systems especially general purpose computers. Therefore, the students are supposed to study, practice and discuss on the major fields discussed in the course to ensure the success of the education process. The outcome of this course implicitly and explicitly affects the abilities the students to understand, analyze and overcome the challenges they face with in the other courses and the real world.

Course Contents:

Module I: Introduction to operating system
Operating system and function, Evolution of operating system, Batch, Interactive, multiprogramming, Time Sharing and Real Time System, multiprocessor system, Distributed system, System protection. Operating System structure, Operating System Services, System Program and calls.

Module II: Process Management
Process concept, State model, process scheduling, job and process synchronization, structure of process management, Threads
Interprocess Communication and Synchronization:
Principle of Concurrency, Producer Consumer Problem, Critical Section problem, Semaphores, Hardware Synchronization, Critical Regions, Conditional critical region, Monitor, Inter Process Communication.
CPU Scheduling:
Job scheduling functions, Process scheduling, Scheduling Algorithms, Non Preemptive and preemptive Strategies, Algorithm Evaluation, Multiprocessor Scheduling.
Deadlock:
System Deadlock Model, Deadlock Characterization, Methods for handling deadlock, Prevention strategies, Avoidance and Detection, Recovery from deadlock combined approach.

Module III: Memory Management
Single Contiguous Allocation: H/W support, S/W support, Advantages and disadvantages, Fragmentation, Paging, Segmentation, Virtual memory concept, Demand paging, Performance, Paged replaced algorithm, Allocation of frames, Thrashing, Cache memory, Swapping, Overlays

Module IV: Device management
Principles of I/O hardware, Device controller, Device Drivers, Memory mapped I/O, Direct Access Memory, Interrupts, Interrupt Handlers, Application I/O interface, I/O Scheduling, Buffering, Caching, Spooling,
Disk organization, Disk space management, Disk allocation Method, Disk Scheduling, Disk storage.

Module V: File System and Protection and security
File Concept, File Organization and Access Mechanism, File Directories, Basic file system, File Sharing, Allocation method, Free space management.
Policy Mechanism, Authentication, Internal excess Authorization.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

Text:

- Milenekovic, “Operating System Concepts”, McGraw Hill
- A. Silberschatz, P.B. Galvin “Operating System Concepts”, John Willey & son

References:

- Dietel, “An introduction to operating system”, Addision Wesley
- Tannenbaum, “Operating system design and implementation”, PHI
- Operating System, A Modern Perspection, Gary Nutt, Pearson Edu. 2000
- A. S Tanenbaum, Modern Operating System, 2nd Edition, PHI.
- Willam Stalling “ Operating system” Pearson Education

COMPUTER ARCHITECTURE

Course Code: ECE2508 **CreditUnits: 03**

Course Objective:
This course deals with computer architecture as well as computer organization and design. Computer architecture is concerned with the structure and behavior of the various functional modules of the computer and how they interact to provide the processing needs of the user. Computer organization is concerned with the way the hardware components are connected together to form a computer system. Computer design is concerned with the development of the hardware for the computer taking into consideration a given set of specifications.

Course Contents:

Module I: Register Transfer Language
Register Transfer, Bus and Memory Transfers, Arithmetic Micro-operations, Logic Micro-operations, Shift Micro-operations, Arithmetic Logic shift Unit.

Module II: Basic Computer Organizations and Design
Instruction Codes, Computer Registers, Computer Instructions, Timing and Control, Instruction Cycle, Memory-Reference Instructions, Input-Output and Interrupt, Design of Accumulator Logic. Hardwired and Microprogrammed control: Control Memory, Address Sequencing, Design of Control Unit

Module III: Central Processing Unit
Introduction, General Register Organization, Stack Organization, Instruction representation, Instruction Formats, Instruction type, Addressing Modes, Data Transfer and Manipulation, Program Control, Reduced Instruction Set Computer RISC and CISC
Computer Arithmetic: Introduction, Multiplication Algorithms, Division Algorithms, Floating-Point Arithmetic Operations

Module IV: Memory and Intrasystem Communication and Input output organisation
Memory: Memory types and organization Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory, Memory Management Hardware

Intrasystem communication and I/O: Peripheral Devices, Input-Output
Controller and I/O driver, IDE for hard disk, I/O port and Bus concept, Bus cycle, Synchronous and asynchronous transfer, Interrupt handling in PC, Parallel Port, RS – 232 interface, Serial port in PC, Serial I/O interface, Universal serial bus IEEE 1394, Bus Arbitration Techniques, Uni-bus and multi-bus architectures EISA Bus, VESA Bus.

Module V: Pipelining, Vector Processing and Multiprocessors
Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processors.
Multiprocessors: Characteristics of Multiprocessors, Interconnection Structures, Interprocessor Arbitration, Interprocessor Communication and Synchronization, Advanced computer architecture, Pentium and Pentinum –Pro, Power PC Architecture

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:

- Morris Mano, Computer System Architecture, 3rd Edition – 1999, Prentice-Hall of India Private Limited.
- Harry & Jordan, Computer Systems Design & Architecture, Edition 2000, Addison Wesley, Delhi.

References:

- WIliam Stallings, Computer Organization and Architecture, 4th Edition-2000, Prentice-Hall of India Private Limited.
- Kai Hwang-McGraw-Hill, Advanced Computer Architecture.
- Kai Hwang & Faye A Briggs, McGrew Hill, inc., Computer Architecture & Parallel Processing.
- John D. Carpinelli, Computer system Organization & Architecture, Edition 2001, Addison Wesley, Delhi
- John P Hayes, McGraw-Hill Inc, Computer Architecture and Organization.
- M.Morris Mano and Charles, Logic and Computer Design Fundamentals, 2nd Edition Updated, Pearson Education, ASIA.
- Hamacher, "Computer Organization," McGraw hill.
- Tennenbaum," Structured Computer Organization," PHI
- B. Ram, "Computer Fundamentals architecture and organization," New age international Gear C. w., "Computer Organization and Programming, McGraw hill

FUZZY LOGIC AND NEURAL NETWORKS

Course Code: ECE2510 **CreditUnits: 02**

Course Objective

Course has been divided in to two parts: Neural Networks and Fuzzy Logic. Neural networks part aims at introducing the fundamental theory and concepts of biological and artificial neural network and their applications in the area of machine intelligence. This part also offers knowledge of learning rules and architecture of various neural nets. The second part covers fuzzy logic: Fuzzy logic is a tool that can be applied to ambiguous problems, which cannot easily solved by classical techniques. Course discusses the fundamental of fuzzy set theory and fuzzy logic. In addition, this course also introduces applications of fuzzy logic in several areas such as fuzzy control and fuzzy decision making.

Course Content:

Module I: Introduction

Biological neurons & memory: structure & function of simple neuron; Artificial Neural Networks (ANN); Typical applications of ANN: Classification, pattern recognition, control, optimization; Basic approach of working on ANN – Training, learning and generalization.

Module II:

Back propagation –architecture –algorithm-derivation of learning rules –number of hidden layers-learningfactors-Hopfield neural net : architecture – algorithm –applications.

Module III:

Neural network based on competition: fixed- weight competitive nets- kohonenself organizing maps andapplications. Adaptive Renonace theory: Basic architecture and operation. Neural controller for a temperature
process.

Module IV:

Basic concepts of fuzzy sets – Relational equation – fuzzy logic control – fuzzification – defuzzification –knowledge base – Decision making logic –membership functions – rule base.

Module V:

Fuzzy logic controller: functional diagram, membership functions: triangular, trapezoidal- scale factors.Fuzzificatoin: membership value assignments using intuition –knowledge base. Defuzzification :maxmembershipprinciple – centeroid method – weighted average method –rule. Choice of variables-derivation ofrules- case study: fuzzy logic controller design for a temperature process

Modes of Evaluation: Quiz/Assignment/ Seminar/Written Examination

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text Books

- Timothy J.Ross, Fuzzy logic with Engineering Applications, McGraw Hill, New york, 1996.
- Kosko.B, Neural Network and fuzzy systems- o\prentice Hall of India Pvt. Ltd., New Delhi, 1992.
- Zurada Jacek M, Introduction to Artificial Neural Systems, West, 1992. (QA76.87.Z96)
- S.N.Shivanandam, S.N.Deepa, Principles of Soft Computing, Wiley 2008

Reference Books

- Neural Networks by Rolf Pfeifer, Dana Damian, Rudolf Fuchslin - University of Zurich.
- Jang Jyh-Shing Roger, Sun Chuen-Tsai and MizutaniEiji, NeuroFuzzy and Soft Computing: A Computational Approach to Learning and Machine Intelligence, Prentice-Hall, 1997.

FUZZY LOGIC AND NEURAL NETWORKS LAB

Course Code: ECE2511 **CreditUnits: 01**

List of Experiments

- To study about MATLAB and learn basic matrix operations.
- Write program to draw straight line, circle and sine functions.
- Study of Biological Neural Network & Artificial Neural Network
- How the weight and bias value effect the output of neuron.
- How weight and bias values are able to represent a decision boundary in feature space.
- Implementation of logic gate (AND,OR,NOT,NAND,NOR) using McCulloh-pitts model.
- How the choice of activation function effects the output of neuron. Experiment with following function: binary threshold and sigmoid function.
- Write a program to implement single layer perception algorithm..
- To Study Fuzzy Logic
- To study and analysis of Fuzzy vs. Crisp logic.
- Write the program to implement various Fuzzy set operations (complement , union, intersection etc.)
- Implementation of fuzzy relations (Max-Min Composition

Modes of Evaluation: Quiz/Assignment/ Seminar/Written Examination

Examination Scheme:

IA				**EE**	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

Syllabus - Sixth Semester

VLSI DESIGN

Course Code: ECE2601 **CreditUnits: 03**

Course Objective:
In the recent years, IC manufacturing technology has gone through dramatic evolution and changes, continuously scaling to ever smatter dimensions. This scaling has a double impact on the design of ICs. First, the complexity of the designs that can be put on a single die has increased dramatically which led to new design methodologies. At the same time, this plunge into deep submicron space causes devices to behave differently and brings challenging issues to forefront. This course along with the course of Digital Circuits and Systems II and Analog CMOS IC design will give you many of the basic essentials to work in the area of Circuit Design. Since this course takes the latest trends in the industry into account, you will find yourself at a definite edge.

Course Contents:

Module I: Devices and the wire
Diode, Dynamic and transient behavior of Diode, Diffusion capacitance, SPICE Diode model, MOSFET basic, depletion and enhancement device.
MOSFET static behavior, Threshold voltage and its dependence on V_{SB} MOSFET Operation in resistive and saturation region, channel length modulation, Velocity saturation and its impact on sub micron devices, sub threshold conduction, Model for manual analysis, Equivalent resistance for MOSFET in (velocity) saturated region, comparison of equations for PMOS and NMOS.
DYNAMIC behavior, Channel capacitance in different regions of operation, junction capacitance, Level 1 SPICE models for MOS transistors.
The Wire, Interconnect parameters: resistance, capacitance and Inductance, Lumped RC model, Elmore Delay

Module II: CMOS Inverter
VTC of an ideal inverter, Switching Model of the CMOS inverter: NMOS /PMOS discharge and charge, VTC of CMOS inverter : PMOS and NMOS operation in various regions including velocity saturation, Switching threshold, (W/L)p/(W/L)n ratio for setting desired V_M with and without velocity saturation, Noise Margins, buffer.
Ratioed logic: Pseudo NMOS inverter and PMOS to NMOS ratio for performance, tri-state inverter, Resistive load inverter.
Load Capacitance calculations: fan out capacitance, self capacitance calculations: Miller effect, wire capacitance; Improving delay calculation with input slope, Propagation delay: first order analysis, analysis from a design perspective, sizing a chain of inverters for minimum delay, choosing optimum number of stages, Power, Energy and Energy Delay: Dynamic power consumption, Static power, Glitches and power dissipation due to direct path currents, power and delay trade off, Transistor sizing for energy minimization

Module III: Combinational circuits
CMOS LOGIC: Good 0 and Poor 0, series and parallel N and P switches, Two and Higher input NAND and NOR gates, Functions of the type (AB+C(D+E)) and their complements, XOR and XNOR gates, 2 input Multiplexer, Full Adder; Transistor sizing in CMOS logic for optimal delay, Pseudo NMOS NAND NOR and other gates and the transistor sizing, Introduction to DSVCL logic, CPL AND/NAND, OR/NOR, XOR/XNOR gates, Logical effort, Electrical Effort, Branching effort, Examples of sizing Combinational logic chains for minimum delay, Pass-transistor logic, pass gate configurations for NMOS and PMOS, 2 input and 4 input MUX, XOR, XNOR and implementation of general functions like AB+AB*C+A*C*, Robust and Efficient PTL Design, Delay of Transmission Gate chain.
Dynamic CMOS design: Pre-charge and Evaluation, charge leakage, bootstrapping, charge sharing, Cascading Dynamic Gates, DOMINO Logic, Optimization of Domino Logic Gates, simple example circuit implementations of DOMINO logic.

Module IV: Sequential Logic circuits
Principle of Bistability, NAND and NOR based SR latch, and clocked SR Latch, JK latch, example of master slave flip flop, CMOS D latch, , MUX based Latches, master slave edge triggered register, Static Timing Analysis –setup, hold time, clock skew, clock period, non ideal clocks, clock overlap, C2MOS register, TSPCR Register, Schmitt Trigger, Pipelining and NORA CMOS

Module V: Layout Design Rules
Introduction to CMOS Process technology, Latch up and its prevention Layout of CMOS inverter, CMOS NAND and NOR gates, Concept of Euler path, and stick diagrams for functions like (AB+E+CD)*

Examination Scheme:

Components	**A**	**CT**	**S/V/Q**	**HA**	**EE**
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
- Jan M Rabaey: Digital Integrated Circuits
- David Hodges et al: Analysis and Design of Digital ICs
- Kang: CMOS Digital ICs
- Weste and Harris: CMOS VLSI design
- Weste and Eshragian: Principles of CMOS VLSI Design

DIGITAL SIGNAL PROCESSING

Course Code: ECE2602 **CreditUnits: 03**

Course Objective:
The objective of the course in Digital signal processing is to provide the student with significant skills in general as well as advanced theories and methods for modification, analysis, detection and classification of analog and digital signals. Furthermore the objective is to give the student a broad knowledge of central issues regarding design, realisation and test of analog and in particular digital signal processing systems consisting of hardware and/or software components. The specialization in signal processing makes it possible to study practical or theoretic fields, ranging from mathematics/signal theory over algorithmic design to development of instruments based on hardware and/or software for real time signal

Course Contents:

Module I: Discrete time signals and systems in time domain
Classification of signal, signal processing operations, classification of systems, discrete time systems, examples of types of signal, sampling process, time domain characterization of LTI discrete- time systems, state space representation of LTI discrete time systems.

Module II: Discrete time signals in transform domain
DTFT, properties, applications, inverse DTFT, DFT, properties, applications, inverse DFT, Z-transform, properties, applications, inverse Z-transform, frequency response, transfer function, Fast Fourier transform algorithms: DIT algorithm, DIF algorithm.

Module III
Discrete time processing of continuous time signals: sampling, analog filter design, antiliasing filter design.

Module IV: Discrete time processing of discrete- time signals
Digital filters: Digital filter structure: FIR filter structure, IIR filter structure
Digital filter design: Impulse invariance method, bilinear transform method of IIR filter design, FIR filter design.

Examination Scheme:

Components	**A**	**CT**	**S/V/Q**	**HA**	**EE**
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

- Prokis, Manolakis: Digital signal processing
- Oppenheim & Schaffer : Digital Signal Processing
- Fafael C. Gonzalez, Richrd E. Woods: Digital Image Processing
- Anil Kumar Jain Fundamentals of Digital Image Processing

ANTENNA AND WAVE PROPOGATION

Course Code: ECE2603 **CreditUnits: 03**

Course Objective:
The purpose of this course is to provide a thorough introduction to antenna systems with an in depth study of various types & performance parameters for antenna.

Course Contents:
Module I: Antenna
Antenna Principles: Potential Functions & Electromagnetic Field, Current Elements, Radiation from Monopole & Half Wave Dipole, power radiated by current element, radiation resistance. Network Theorems, Directional Properties of Dipole Antenna. Antenna Gain, Effective Area, Antenna Terminal Impedance, Practical Antennas and Methods of Excitation, Antenna Temperature and Signal to Noise Ratio.

Module II: Antenna Arrays
Antennas Arrays: Two Element Array, Horizontal Patterns in Broadcast Arrays, Linear Arrays, Multiplication of patterns, effect of the earth on vertical patterns, Binomial array

Module III: Wave Propagation
Modes of Propagation, Plane Earth Reflection, Space wave and Surface Wave, Reflection and refraction waves by the Ionosphere Tropospheric Wave. Ionosphere Wave Propagation in the Ionosphere, Virtual Height, MUF Critical frequency, Skip Distance, Duct Propagation, Space wave

Module IV:Practical Antennas
VLF and LF transmitting antennas, effect of antenna height, Field of short dipole, electric field of small loop antenna, Directivity of circular loop antenna with uniform current, Yagi-Uda array: Square corner yagi-uda hybrid, circular polarization Rhombic Antenna: Weight and Leg length Parabolic Reflectors: Properties, Comparison with corner reflectors Horn Antenna: Length and Aperture. Introduction to Turstile Antenna Effect of ground on antenna performance.
Broadband Antenna: Frequency independent concept, RUMSEY's Principle, Frequency independent planar log spiral antenna, Frequency independent conical spiral Antenna.

Module V: Antenna Measurements
Radiation Pattern measurement, Distance requirement for uniform phase, uniform field amplitude requirement, Introduction to phase measurement; Gain Measurement: Comparison method, Near field method, Introduction to current distribution measurement, Measurement of antenna efficiency, measurement of Noise figure and noise temperature of an antenna polarization measurement.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:
- Jordan Edwards C. and Balmain Keith G.S "Electromagnetic Waves and Radiating Systems"/ Prentice Hall (India)
- Kraus, John D. &Mashefka, Ronald J. / "Antennas: For All Applications" / Tata McGraw Hill, 3rd Ed.

References:
- Prasad, K.D./ "Antennas and Wave Propagation"/ Khanna Publications
- Collin, R. / "Antennas and Radiowave Propagation" / Tata McGraw-Hill
- Hayt Jr. William H./ "Engineering Electromagnetic "/ Tata McGraw-Hill
- Das, Annaparna& Das, Sisir K. / "Microwave Engineering"/ Tata McGraw Hill.
- Roy, Sitesh Kumar &Mitra, Monojit / "Microwave Semiconductor Devices" / Prentice Hall (India)

RADAR AND SATELLITE COMMUNICATION

Course Code: ECE2611 **CreditUnits: 03**

Course Objective:
This course builds basic knowledge of different types of Radar systems and satellite communication along with link designing & application. It also covers different modulation schemes & channels used.

Course Contents:

Module I: Introductionto Radar
Principle of detection and ranging, Radar frequencies and bands. Applications, Radar block diagram and operation. Radar Range Equation : Range prediction, Minimum detectable signal, Receiver noise SNR, Integration of radar pulses, Radar cross section of targets, Transmitter Power, PRF and system losses & Propagation effects.

Module II: CW FM Radar
Doppler effect, CW Radar, Frequency-modulated CW Radar, Multiple-frequency CW Radar. MTI and Pulse Doppler Radar: MTI delay lines, Delay line Cancellers, Coherent and Non-Coherent MTI, Pulse Doppler Radar.

Module III: Introduction to Satellite
Communication satellites, Orbiting satellites, Frequencies and bands, Satellite multiple access formats. Satellite Channel: Power flow, Polarization, Atmospheric losses, Receiver noise, CNR, Satellite link analysis for uplinks and downlinks. Overview of Coaxial cable system and optical Network (SONET); Overview of WLL (Wireless loop)

Module IV: Satellite Transponder
Transponder model, Satellite signal processing RF-RF translation, IF demodulation.

Module V: Multiple-Access
FDMA; amplification with multiple FDMA carriers, AM/FM Conversion with FDMA, Switched FDMA, Synchronization, SS-TDMA; CDMA; DS CDMA, Frequency- hopped, CDMA. Carrier recovery & bit timing. Satellite link budget analysis

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
- Introduction to Radar Systems - M.I. Skolnik
- Radar Fundamentals - G.J. Wheeler.
- Radar Engineering - D.G. Rink
- Satellite Communication - R.M. Gagliardi
- Satellite Communication - T. Pratt & C.W. Boston
- Satellite Communication System Design Principles - M. Richharia

VLSI DESIGN LAB

Course Code: ECE2605 **CreditUnits: 01**

Course Contents:

1. MOSFET characteristics with varying V_{GS} for both pmos and nmos.
2. Effect on VTC of CMOS inverter with variation of W and L.
3. Transient analysis of CMOS inverter with varying capacitive load, W and L.
4. Rise time, Fall time power dissipation, propagation delay calculation of CMOS inverter with the variation ofcapacitive load, W and L.
5. NOR and NAND gate - Transient analysis
6. XOR/XNOR gate - Transient analysis
7. 2:1 MUX and XOR gate with P.T.L.- Transient analysis
8. D type latch and flip flop - Transient analysis
9. 3 input NAND gate implementation with DOMINO (precharge and evaluation)
10. 4 inverter chain to derive capacitive load

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

DIGITAL SIGNAL PROCESSING LAB

Course Code: ECE2609 **CreditUnits: 01**

List of Experiments:

- To generate unit step sequence, exponential sequence and sinusoidal sequence
- To determine convolution of two given sequences.
- To plot the frequency response of an FIR system
- To compute DFT and IDFT of a given sequence
- To determine the circular convolution of two given sequences
- To design various analog filters
- To design FIR filter using Hamming window
- To convert Analog filter into Digital Filter using bilinear transformation
- To determine z and inverse z transform of a given sequence
- To verify 8 points FFT algorithm in decimation in time (DIT) & decimation in frequency (DIF).
- To determine the filter coefficient using Ramez exchange algorithm.
- To design an IIR digital filter and its parallel realization.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

RADAR AND SATELLITE COMMUNICATIONS LAB

Course Code: ECE2612 **CreditUnits: 01**

Course Contents:

1. To study AM transmitter and receiver.

2. To study FM transmitter and receiver.

3. To implement the following circuits.
   - AM Transmitter
   - FM Transmitter
   - AM Receiver
   - FM Receiver
   - Remote Control
   - Wireless Mic System

4. To study RF portion of satellite receiver.
   - Study of dish antenna and section N.B section
   - Study of tuner
   - Study of R.F modulator section

5. To study the base-band portion of satellite receiver
   - study of video section
   - study of sound section
   - study of signal indictor
   - study of power supply section

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

ADVANCED JAVA PROGRAMMING

Course Code: ECE2607 **CreditUnits: 02**

Course Objective:
The objective is to equip the students with the advanced feature of contemporary java which would enable them to handle complex programs relating to managing data and processes over the network. The major objective of this course is to provide a sound foundation to the students on the concepts, precepts and practices, in a field that is of immense concern to the industry and business.

Course Contents:

Module I
Introduction to Java RMI, RMI services, RMI client, Running client and server, Introduction of Swing, Swing Components, Look and Feel for Swing Components, Introduction to Multimedia Programming.

Module II
ODBC and JDBC Drivers, Connecting to Database with the java.sql Package, Using JDBC Terminology; Evolving Nature of Area

Module III
Introduction to Servlets, Servlet Life Cycle, Servlet based Applications, Servlet and HTML. JSP: Introduction to JSP, JSP implicit objects, JSP based Applications

Module IV
Enterprise Java Beans:-EJB roles—EJB Client-Object -container-Transaction Management—implementing a Basic EJB Object-Implementing session Beans-Implementing Entity Beans-Deploying an enterprise Java Beans Object-Changes in EJB1.1 specification.

Module V
The Model-View-Controller Architecture What is Struts, Struts Tags, Creating Beans, Other Bean Tags, Bean Output, Creating HTML Forms, The ActionForm class The Action class, SimpleStruts: a simple Struts application

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:
- Java 2 Unleashed (Techmedia – SAMS), Jamie Jaworski
- Professional Java Server Programming (a Press), Allamaraju
- Developing Java Servlets (Techmedia – SAMS), James Goodwill
- Using Java 1.2 Special Edition (PHI), Webber

References:
- David Flanagan, Jim Parley, William Crawford & Kris Magnusson , Java Enterprise in a nutshell- A desktop Quick reference - O'REILLY, 2003
- Stephen Ausbury and Scott R. Weiner, Developing Java Enterprise Applications, Wiley-2001
- JaisonHunder& William Crawford, Java Servlet Programming, O'REILLY, 2002
- Dietal and Deital, "JAVA 2" PEARSON Publication

ADVANCED JAVA PROGRAMMING LAB

Course Code: ECE2610 **CreditUnits: 01**

Programming Language: Java

1. WAP to display label and a button on a frame with the help of JFrame
2. WAP to display six buttons on a panel using JFrame.
3. WAP that implement a JApplet that display a simple label
4. WAP that implement a JApplet and display the frame with options to enter data for following fields:
    a. Customer name
    b. Customer number
    c. Age
    d. Address
5. WAP to implement a simple client/server, RMI based Application.
6. WAP to create and implement a TCP/IP socket based Application.
7. WAP that implement a simple servlet program.
8. WAP for authentication, which validate the login-id and password by the servlet code.
9. WAP to connect a database using user-id and password.
10. WAP to insert data into the database using the prepared statement.
11. WAP to read data from the database using the Resulset.
12. WAP to read data send by the client (HTML page) using servlet.
13. WAP to include a HTML page into a JSP page.
14. WAP to read data send by a client (HTML page) using JSP.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

EMBEDDED SYSTEM

Course Code: ECE2613 **CreditUnits: 02**

Course Objective : The objective of this course is to provide the knowledge of 8051 microcontroller and with a basic understanding of instruction sets & assembly language programming. Programming the microcontroller in 8051 C is also emphasized in the course.

Course Contents:

Module-I: Introduction to an embedded systems design & RTOS
Introduction to Embedded system, Processor in the System, Microcontroller, Memory Devices, Embedded System Project Management, ESD and Co-design issues in System development Process, Design cycle in the development phase for an embedded system, Use of target system or its emulator and In-circuit emulator, Use of software tools for development of an ES. Inter-process Communication and Synchronization of Processes, Tasks and Threads, Problem of Sharing Data by Multiple Tasks, Real Time Operating Systems: OS Services, I/O Subsystems, and Interrupt Routines in RTOS Environment, RTOS Task Scheduling model, Interrupt Latency and Response times of the tasks.

Module-II: Overview of Microcontroller
Microcontroller and Embedded Processors, Overview of 8051 Microcontroller family: Architecture, basic assembly language programming concepts, The program Counter and ROM Spaces in the 8051, Data types, 8051 Flag Bits ad PSW Register, 8051 Register Banks and Stack Instruction set, Loop and Jump Instructions, Call Instructions, Time delay generations and calculations, I/O port programming Addressing Modes, accessing memory using various addressing modes, Arithmetic instructions and programs, Logical instructions, BCD and ASCII application programs, Single-bit instruction programming, Reading input pins vs. port Latch, Programming of 8051 Timers, Counter Programming.

Module-III: Communication with 8051
Basics of Communication, Overview of RS-232, I2C Bus, UART, USB, IEEE 488 (GPIB). Parallel input output applications. (Stepper motor Sequencer program, Strobed input/output). Interrupt driven applications (real time clock, serial input/output with interrupt). Analog-digital interfacing (Pulse width modulator, 8-bit ADC).

Module-IV: Basics of 8051 C Programming
Introduction to 8051 C, 8051 memory constitution, Constants, variables and data types. Arrays structures and unions, pointers, Loops and decisions, Functions, Modules and programs.

Module-V: 8051 C Programming
Data interface, Timer control, Interrupt operations, Digital operations, A/D and D/A conversions, Common control problem examples (Centronics parallel interface, Printer interface, Memory access, Key matrix scanning, Stepper motor control and digital clock.).

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination, A: Attendance

Text Books

- Raj Kamal, "Embedded Systems", Tata McGraw-Hill, 2004
- James W. Stewart and Kai X. Miao, "The 8051 microcontroller", Pearson Education Prentice Hall, 2nd Edition 2008
- M.A. Mazidi and J. G. Mazidi, "The 8051 Microcontroller and Embedded Systems", Prentice-Hall, 2004

Reference Books

- David E. Simon, “An Embedded Software Primer”, Pearson Education, 1999
- K.J. Ayala, “The 8051 Microcontroller”, Penram International, 1999
- Dr. Rajiv Kapadia, “8051 Microcontroller & Embedded Systems”, Jaico Press, 2004
- Dr. Prasad, “Embedded Real Time System”, Wiley Dreamtech press, 2004

EMBEDDED SYSTEM LAB

Course Code: ECE2614 **CreditUnits: 01**

Course Content

- WAP to add two 8-bit numbers using microcontroller 8051.
- WAP to multiply two 8-bit numbers using microcontroller 8051.
- WAP to divide two 8-bit numbers using microcontroller 8051.
- WAP to subtract two 8-bit numbers using microcontroller 8051.
- WAP to generate a geometric progression using microcontroller 8051.
- WAP to generate a square wave using microcontroller 8051.
- WAP to generate a delay of 5 ms using microcontroller 8051.
- Study and implement serial communication by interfacing microcontroller with a computer.
- Study and implement parallel data communication by interfacing microcontroller with a LCD.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

Syllabus - Seventh Semester

MICROWAVE ENGINEERING

Course Code: ECE2703 **CreditUnits: 03**

Course Objective:
This course deals with the microwaves. Microwaves are important when we are going to the high frequency regime. By studying this course students will be able to know about the microwave components and devices, microwave generators and their characteristics, microwave applications and measurement. Also they will be familier about the rectangular and circular waveguides, their equations and the modes existing in these waveguides.

Course Contents:

Module I: Introduction
Microwave frequencies, standard frequency bands, behaviour of circuits at conventional and microwave frequencies, microwave application.

Module II: Waveguide
Overview of guided waves, TE, TM and TEM modes, rectangular and cylindrical wave guide resonators, choice of the type of waveguide, waveguide problems.

Module III: Microwave Components and Devices
Scattering matrix and its properties, coupling probes, coupling loops, windows, waveguide tuners, termination, E-plane Tee, H-plane Tee, Magic Tee, Phase-Shifter, attenuators, Directional Coupler, Gunn diode, Resonator and circulators, IMPATT devices, TRAPATT.

Module IV: Microwave tubes
Transit-time effect, limitations of conventional tubes, Two-cavity and multi-cavity Klystrons, Reflex Klystron, TWT and Magnetrons.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
- Microwave Devices and Circuits, Liao
- Microwave Principles, Herbert J Reich
- Microwaves, K.C. Gupta
- Microwave Techniques , D C Agrawal
- Elements of Microwave Engg, Chatterjee

MOBILE COMMUNICATION

Course Code: ECE2708 **CreditUnits: 02**

Course Objective:
This course introduce about global system for mobile, 2.5G, 3G technologies, how wireless communication system works and what is FDMA, TDMA. This course also introduce some facts about propagation models.

Course Contents:

Module I: Introduction to Wireless Communication System
Evolution of mobile radio communication, Mobile radiotelephony in U.S., Mobile radio system around the world, second generation (2G) cellular network , evolution to 2.5G wireless network , evolution for 2.5G TDMA standards, third generation (3G) wireless network.

Module II: The Cellular Concept
System design fundamentals, frequency reuse channel assignment strategies, Hand off strategies, Interference and system capacity, improving coverage and capacity in cellular system.

Module III: Propagation Model and Spread Spectrum Modulation Techniques
Longley rice model, okumara model, hata model, pcs extension to hata model, wolfish and bertoni model, Pseudo Noise (PN) sequence, Direct sequence spread spectrum (DSSS), frequency hopped spread spectrum (FHSS).

Module IV: Multiple Access Techniques for Wireless Communication
Introduction to multiple access, Frequency division multiple access (FDMA), Time division Multiple access (TDMA), Spread spectrum multiple access, Packet Radio.

Module V: Global System for Mobile
Global system for mobile (GSM), GSM system architecture, GSM radio subsystem, GSM channel types, Example of a GSM cell, Frame structure of GSM.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:
- Wireless Communications, Theodore S. Rappaport

References:
- Wireless Communications & Networks by William Stallings.
- Wireless Intelligent Networking by Gerry Christensen, Robert Duncan, Paul G. Florack

MEASURMENT AND MEASURING INSTRUMENTS

Course Code: ECE2714 **CreditUnits: 03**

Course Objective:
The objective of the course is to provide a brief knowledge of measurements and measuring instruments related to engineering. The basic idea of this course is to give the sufficient information of measurements in any kind of industry viz. electrical, electronics, mechanical e t c.

Course Contents:

Module I: Theory of Measurement
Introduction, Unit System, Performance Characteristics: static & dynamic standards, Error analysis: Sources, types and statistical analysis.

Module II: Transducers
Passive transducers, Active transducers: Classification, selection, Measurement of Pressure, Strain, Resistance, Capacitance and inductance. strain gauges, rossettes, LVDT, interfacing resistive transducers to electronic circuits.

Module III: Analog Meters
AC analog meter: Average, Peak and RMS voltmeters, sampling voltmeters. Electronics Analog meters: Electronics analog DC and AC voltmeter and ammeters, ohmmeter and multimeter

Module IV: Data Acquisition System
Introduction to data acquisition systems, Bridges: Wheatstone's bridge, Kelvin double bridge; Megger; Andersons Bridge; Schering Bridge; sources and detectors, shielding of bridges.

Module V: Digital Meters and Oscilloscopes
Display devices: Decimal, BCD and straight binary number, indicating system, numeric & alpha number display using LCD & LED, specification of digital meters: display digit & counts resolution, sensitivity, accuracy, speed & settling time etc.
Types of oscilloscopes, Measurement of Frequency.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:
- Electronic Instrumentation Technology by MMS Anand, PHI Pvt. Ltd., New Delhi Ed. 2005.
- Electronics Instrumentation by H.S. Kalsi TMH Ed. 2004.

References:
- Electronics Instrumentation & Measurement Techniques by W.D. Cooper & A.D. Helfrick, PHI 3rd Ed.
- Electronics Measurement & Instrumentation by Oliver & Cage Mc-Graw Hill.

MICROWAVE ENGINEERING LAB

Course Code: ECE2705 **CreditUnits: 01**

List of Experiments:

1. To study the characteristics of reflex klystron.
2. To study the characteristic of Gunn diode.
3. To measure frequency and guided wavelength of a microwave signal.
4. To measure the impedance of a given load.
5. To measure the dielectric constant of the given sample.
6. To measure various parameters of a directional coupler.
7. To study the characteristic and functions of an isolator.
8. To study the characteristic and functions of a circulator.
9. To study the characteristic and functions of various tees.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

MEASURMENT AND MEASURING INSTRUMENTS LAB

Course Code: ECE2715 **CreditUnits: 01**

Course Contents:

1. Measurement of resolution and sensitivity of thermocouple (study of various thermocouples J, K, T, etc.) (Calibration)
2. Measurement of resolution, sensitivity and non linearity of thermistor (thermistor instability)
3. Measurement of thickness of LVDT.
4. Measurement of resolution of LVDT (and displacement measurement)
5. Study of proportional control and offset Problems.
6. Study of proportional integral control.
7. Study of proportional integral derivative (PID) control.
8. Vibration measurement by stroboscope (natural frequency of a cantilever)
9. Angular frequency (speed of rotating objects) measurement by stroboscope.
10. Pressure transducer study and calibration.
11. Proving ring (force measurement)

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

SUMMER INTERNSHIP EVALUATION-II

Course Code: ECE2735 **CreditUnits: 03**

Methodology:

Practical training is based on the theoretical subjects studied by students. It can be arranged within the college or in any related industrial unit. The students are to learn various industrial, technical and administrative processes followed in the industry. In case of on-campus training the students will be given specific task of fabrication/assembly/testing/analysis. On completion of the practical training the students are to present a report covering various aspects learnt by them and give a presentation on same.

Examination Scheme:

Feedback from industry/work place	20
Training Report	40
Viva	15
Presentation	25
Total	**100**

OPTICAL COMMUNICATION

Course Code: ECE2706 **CreditUnits: 02**

Course Objective:
The objective of this course is to introduce the student to the fundamental basics and understanding of fiber optical communication. This includes the properties of optical fibers and how are they used to establish optical links for communication systems.

Course Contents:

Module I: Fundamentals of Fiber Optics
Different generations of optical fiber communication systems, Optical fiber structure, light propagation-total internal reflection, acceptance angle and numerical aperture, signal attenuation and dispersion. Modes in an optical fiber, Optical fibers: step-index, Graded-index, Single and Multimode, other types of fibers.

Module II: Optical Sources
LED-spontaneous emission- material used in LED, LED efficiency, surface emitting LED, edge emitters, stimulated emission, spontaneous emission, Structure of various LED's, LASER: stimulated emission, double heterostructure LASER, LASER tuning and degradation, driver for LED and LASER.

Module III: Photo Detectors
Characteristics of photo detector, direct and indirect band gap semiconductors, homo junction and hetro junction photodiodes, p-i-n photodiode, avalanche photodiode, phototransistor, optocouplers.

Module IV: Fiber Properties
Fiber end preparation, fiber splicing, fiber connectors, connection losses, fiber couplers, fiber materials, fiber fabrication, mechanical properties of fibers, different fiber cables.

Module V: Fiber Optic Communication System
Basic communication components, coupling to and from the fiber, multiplexing and coding , repeaters, bandwidth and rise time budgets, noise, bit error rate and eye pattern.

Module VI: Application of Fiber Optics
Long haul communication, LAN, medical application, undersea communication, military application, coherent optical communication, Fiber optic sensors- Intensity modulated sensor, Phase sensor, Diffraction Grating sensors.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

- J M Senior : Optical fiber Communication
- Keiser: Optical communication
- Myanbaev and Scheiner: Fiber-Optic Communications Technology

OPTICAL COMMUNICATIONS LAB

Course Code: ECE2716 **CreditUnits: 01**

Course Contents:

- To study LASER free space Communication.
- To study losses in optical fiber.
- To measure the Numerical Aperture of the Fiber.
- To characterize optical sources.
- Design and evaluation of LD digital transmission system.
- To study video transmission through optical fiber link.
- To study WDM in optical fibers.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

SOFTWARE ENGINEERING

Course Code: ECE2707 **CreditUnits: 03**

Course Objective:
The basic objective of Software Engineering is to develop methods and procedures for software development that can scale up for large systems and that can be used to consistently produce high-quality software at low cost and with a small cycle time. Software Engineering is the systematic approach to the development, operation, maintenance, and retirement of software.
The course provides a thorough introduction to the fundamentals principles of software engineering. The organization broadly be based on the classical analysis-design-implementation framework.

Course Contents:
Module I: Introduction
Software life cycle models: Waterfall, Prototype, Evolutionary and Spiral models, Overview of Quality Standards like ISO 9001, SEI-CMM

Module II: Software Metrics and Project Planning
Size Metrics like LOC, Token Count, Function Count, Design Metrics, Data Structure Metrics, Information Flow Metrics. Cost estimation, static, Single and multivariate models, COCOMO model, Putnam Resource Allocation Model, Risk management.

Module III: Software Requirement Analysis, design and coding
Problem Analysis, Software Requirement and Specifications, Behavioural and non-behavioural requirements, Software Prototyping Cohesion & Coupling, Classification of Cohesiveness & Coupling, Function Oriented Design, Object Oriented Design, User Interface Design Top-down and bottom-up Structured programming, Information hiding,

Module IV: Software Reliability, Testing and Maintenance
Failure and Faults, Reliability Models: Basic Model, Logarithmic Poisson Model, Software process, Functional testing: Boundary value analysis, Equivalence class testing, Decision table testing, Cause effect graphing, Structural testing: path testing, Data flow and mutation testing, unit testing, integration and system testing, Debugging, Testing Tools, & Standards.Management of maintenance, Maintenance Process, Maintenance Models, Reverse Engineering, Software RE-engineering

Module V: UML
Introduction to UML, Use Case Diagrams, Class Diagram: State Diagram in UMLActivity Diagram in UMLSequence Diagram in UMLCollaboration Diagram in UML

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:

- K. K. Aggarwal & Yogesh Singh, "Software Engineering", 2nd Ed, New Age International, 2005.
- R. S. Pressman, "Software Engineering – A practitioner's approach", 5th Ed., McGraw Hill Int. Ed., 2001.

References:

- R. Fairley, "Software Engineering Concepts", Tata McGraw Hill, 1997.
- P. Jalote, "An Integrated approach to Software Engineering", Narosa, 1991.
- Stephen R. Schach, "Classical & Object Oriented Software Engineering", IRWIN, 1996.
- James Peter, W. Pedrycz, "Software Engineering", John Wiley & Sons.
- Sommerville, "Software Engineering", Addison Wesley, 1999.
- Sommerville, "Software Engineering", Addison Wesley, 1999.

DIGITAL IMAGE PROCESSING

Course Code: ECE2712 **CreditUnits: 02**

Course Objective:
The syllabus is divided into four parts, the first one deal with introduction and fundamental concepts of digital image processing and image enhancement in spatial domain. Second module of the syllabus deals with image processing operations like image enhancement in frequency domain, image restoration respectively. Third and fourth module deals with applications like Image Compression and Object recognition respectively The syllabus helps a student perfect image processing fundamentals. Apart from it image processing application are discussed in detail.

Course Contents:
Module I: Introduction and Digital Image Fundamentals
The origins of Digital Image Processing, Examples of Fields that Use Digital Image Processing, Fundamentals Steps in Image Processing, Elements of Digital Image Processing Systems, Image Sampling and Quantization, Some basic relationships like Neighbors, Connectivity, Distance Measures between pixels, Linear and Non Linear Operations.
Image Enhancement in the Spatial Domain: Some basic Gray Level Transformations, Histogram Processing, Enhancement Using Arithmetic and Logic operations, Basics of Spatial Filters, Smoothening and Sharpening Spatial Filters, Combining Spatial Enhancement Methods.

Module II: Image Enhancement in the Frequency Domain
Introduction to Fourier Transform and the frequency Domain, Smoothing and Sharpening Frequency Domain Filters, Homomorphic Filtering.
Image Restoration: A model of The Image Degradation / Restoration Process, Noise Models, Restoration in the presence of Noise Only Spatial Filtering, Pereodic Noise Reduction by Frequency Domain Filtering, Linear Position-InvarientDedradations, Estimation of Degradation Function, Inverse filtering, Wiener filtering, Constrained Least Square Filtering, Geometric Mean Filter, Geometric Transformations.

Module III: Image Compression
Coding, Interpixel and Psychovisual Redundancy, Image Compression models, Elements of Information Theory, Error free comparison, Lossy compression, Image compression standards.
*Image Segmentation:*Detection of Discontinuities, Edge linking and boundary detection, Thresholding, Region Oriented Segmentation, Motion based segmentation

Module IV: Representation and Description
Representation, Boundary Descriptors, Regional Descriptors, Use of Principal Components for Description, Introduction to Morphology, Some basic Morphological Algorithms.
Object Recoginition: Patterns and Pattern Classes, Decision-Theoretic Methods, Structural Methods.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:
- Rafael C. Conzalez& Richard E. Woods, 2002, "Digital Image Processing", 2nd edition, Pearson Education.
- A.K. Jain, 1989, "Fundamental of Digital Image Processing", PHI.

References:
- Bernd Jahne, 2002, "Digital Image Processing", 5th Ed., Springer.
- William K Pratt, 2001, "Digital Image Processing: Piks Inside", John Wiley & Sons.

DIGITAL IMAGE PROCESSING LAB

Course Code: ECE2713 **CreditUnits: 01**

List of Assignments:

Experiments will be based on Image Representation, Image transformation, Image Enhancements, Edge Detection, Morphological Image processing and Segmentation.

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

COMPUTER NETWORKS

Course Code: ECE2717 **CreditUnits: 03**

Course Objective:
The objective is to acquaint the students with the basics of data communication and networking. A structured approach to explain how networks work from the inside out is being covered. The physical layer of networking, computer hardware and transmission systems have been explained. In-depth application coverage includes email, the domain name system; the World Wide Web (both client- and server-side); and multimedia (including voice over IP.

Course Contents:

Module I: Introduction
Introduction to computer networks, evolution of computer networks and its uses, reference models-OSI Model, TCP/IP model, example networks
The physical layer: Theoretical basis for data communication, transmission media, wireless transmission, telecom infrastructure, PSTN, communication satellites, mobile telephone system

Module II: The data link layer
Data link layer design issues, error detection and correction, data link protocols, sliding window protocols, example of data link protocols- HDLC, PPP Access

Module III: Medium access layer
Channel allocation problem, multiple access protocols, ALOHA, CSMA/CD, CSMA/CA, IEEE Standard 802 for LAN and MAN, Bridges, Wireless LANs. Introduction to wireless WANs: Cellular Telephone and Satellite Networks, SONETISDH, Virtual-Circuit Networks: Frame Relay and ATM.

Module IV: The network layer
Network layer concepts, design issues, static and dynamic routing algorithms, shortest path routing, flooding, distance vector routing, link state routing, multicast routing, congestion control and quality of service, internetworking (IPv6), Ipv4

Module V: The transport layer
The transport services, elements of transport protocols, TCP and UDP
The application layer: Brief introduction to presentation and session layer, DNS,E-mail**,** WWW

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:
- Computer networks: Tanenbaum, Andrew S, Prentice Hall
- Data communication &neworking: Forouzan, B. A.

References:
- Computer network protocol standard and interface: Uyless, Black
- Data and Computer Communications, Seventh Edition (7th.) William Stallings Publisher: Prentice Hall
- Computer Networking: A Top-Down Approach Featuring the Internet (3rd Edition) by James F. Kurose

INDEPENDENT STUDY

Course Code: ECE2718 **CreditUnits: 02**

This is an elective, self-directed course to investigate a emerging areas of IT and Computer Science like Mobile Operating System, Cloud Computing, or from Current Research Areas etc. The primary goal of the course is to provide students with research exploration of a specific topic of interest to the individual student under the advisement of an instructor who will monitor and critique the student's progress.

Independent study provides students with the opportunity to work one-on-one with a Faculty on a particular topic. The student and faculty should discuss the aims and content of the study and present the proposal to Head of Department. The independent study proposal should include the study's title, theme, readings, work to be submitted, and syllabus. Faculty and student should meet for a minimum number of 2 hours per week. Student will give a seminar after completion of study.

TERM PAPER

Course Code: ECE2731 **CreditUnits: 02**

A term (or research) paper is primarily a record of intelligent reading in several sources on a particular subject.
The students will choose the topic at the beginning of the session in consultation with the faculty assigned. The progress of the paper will be monitored regularly by the faculty. At the end of the semester the detailed paper on the topic will be submitted to the faculty assigned. The evaluation will be done by Board of examiners comprising of the faculties.

GUIDELINES FOR TERM PAPER
The procedure for writing a term paper may consist of the following steps:
1. Choosing a subject
2. Finding sources of materials
3. Collecting the notes
4. Outlining the paper
5. Writing the first draft
6. Editing & preparing the final paper

1. Choosing a Subject
The subject chosen should not be too general.

2. Finding Sources of Materials
a) The material sources should be not more than 10 years old unless the nature of the paper is such that it involves examining older writings from a historical point of view.
b) Begin by making a list of subject-headings under which you might expect the subject to be listed.
c) The sources could be books and magazine articles, news stories, periodicals, scientific journals etc.

3. Collecting the notes
Skim through sources, locating the useful material, then make good notes of it, including quotes and information for footnotes.
a) Get facts, not just opinions. Compare the facts with author's conclusion.
b) In research studies, notice the methods and procedures, results & conclusions.
c) Check cross references.

4. Outlining the paper
a) Review notes to find main sub-divisions of the subject.
b) Sort the collected material again under each main division to find sub-sections for outline so that it begins to look more coherent and takes on a definite structure. If it does not, try going back and sorting again for main divisions, to see if another general pattern is possible.

5. Writing the first draft
Write the paper around the outline, being sure that you indicate in the first part of the paper what its purpose is. You may follow the following:
a) statement of purpose
b) main body of the paper
c) statement of summary and conclusion
Avoid short, bumpy sentences and long straggling sentences with more than one main idea.

6. Editing &Preparing the final Paper
a) Before writing a term paper, you should ensure you have a question which you attempt to answer in your paper. This question should be kept in mind throughout the paper. Include only information/ details/ analyses of relevance to the question at hand. Sometimes, the relevance of a particular section may be clear to you but not to your readers. To avoid this, ensure you briefly

explain the relevance of every section.

b) Read the paper to ensure that the language is not awkward, and that it "flows" properly.
c) Check for proper spelling, phrasing and sentence construction.
d) Check for proper form on footnotes, quotes, and punctuation.
e) Check to see that quotations serve one of the following purposes:
   (i) Show evidence of what an author has said.
   (ii) Avoid misrepresentation through restatement.
   (iii) Save unnecessary writing when ideas have been well expressed by the original author.
f) Check for proper form on tables and graphs. Be certain that any table or graph is self-explanatory.

Term papers should be composed of the following sections:

1) Title page
2) Table of contents
3) Introduction
4) Review
5) Discussion&Conclusion
6) References
7) Appendix

Generally, the introduction, discussion, conclusion and bibliography part should account for a third of the paper and the review part should be two thirds of the paper.

Discussion

The discussion section either follows the results or may alternatively be integrated in the results section. The section should consist of a discussion of the results of the study focusing on the question posed in the research paper.

Conclusion

The conclusion is often thought of as the easiest part of the paper but should by no means be disregarded. There are a number of key components which should not be omitted. These include:

a) summary of question posed
b) summary of findings
c) summary of main limitations of the study at hand
d) details of possibilities for related future research

Reference

From the very beginning of a research project, you should be careful to note all details of articles gathered.
The bibliography should contain ALL references included in the paper. References not included in the text in any form should NOT be included in the bibliography.
The key to a good bibliography is consistency. Choose a particular convention and stick to this.

Conventions

Monographs
Crystal, D. (2001), Language and the internet. Cambridge: Cambridge University Press.

Edited volumes

Gass, S./Neu, J. (eds.) (1996), Speech acts across cultures. Challenges to communication in a second language. Berlin/ NY: Mouton de Gruyter.
[(eds.) is used when there is more than one editor; and (ed.) where there is only one editor. In German the abbreviation used is (Hrsg.) for Herausgeber].

Edited articles

Schmidt, R./Shimura, A./Wang, Z./Jeong, H. (1996), Suggestions to buy: Television commercials from the U.S., Japan, China, and Korea. In: Gass, S./Neu, J. (eds.) (1996), Speech acts across cultures. Challenges to communication in a second language. Berlin/ NY: Mouton de Gruyter: 285-316.

Journal articles
McQuarrie, E.F./Mick, D.G. (1992), On resonance: A critical pluralistic inquiry into advertising rhetoric. Journal of consumer research 19, 180-197.

Electronic book
Chandler, D. (1994), Semiotics for beginners [HTML document]. Retrieved [5.10.'01] from the World Wide Web, http://www.aber.ac.uk/media/Documents/S4B/.

Electronic journal articles
Watts, S. (2000) Teaching talk: Should students learn 'real German'? [HTML document]. German as a Foreign Language Journal [online] 1. Retrieved [12.09.'00] from the World Wide Web, http://www.gfl-journal.com/.

Other websites
Verterhus, S.A. (n.y.), Anglicisms in German car advertising. The problem of gender assignment [HTML document]. Retrieved [13.10.'01] from the World Wide Web, http://olaf.hiof.no/~sverrev/eng.html.

Unpublished papers
Takahashi, S./DuFon, M.A. (1989), Cross-linguistic influence in indirectness: The case of English directives performed by native Russian speakers. Unpublished paper, Department of English as a Second Language, University of Hawai'i at Manoa, Honolulu.

sUnpublished theses/ dissertations
Möhl, S. (1996), Alltagssituationen im interkulturellen Vergleich: Realisierung von Kritik und Ablehnung im Deutschen und Englischen. Unpublished MA thesis, University of Hamburg.
Walsh, R. (1995), Language development and the year abroad: A study of oral grammatical accuracy amongst adult learners of German as a foreign language. Unpublished PhD dissertation, University College Dublin.

Appendix
The appendix should be used for data collected (e.g. questionnaires, transcripts, ...) and for tables and graphs not included in the main text due to their subsidiary nature or to space constraints in the main text.

Assessment Scheme:

Continuous Evaluation: (Based on abstract writing, interim draft, general approach, research orientation, readings undertaken etc.)	40%
Final Evaluation: (Based on the organization of the paper, objectives/ problem profile/ issue outlining, comprehensiveness of the research, flow of the idea/ ideas, relevance of material used/ presented, outcomes vs. objectives, presentation/ viva etc.)	60%

PROJECT

Course Code: ECE2732 **CreditUnits: 02**

Course Objective:
The objective of this course is to provide practical training on some live/demo projects that will increase capability to work on actual problem in industry. It will be an in house training on some latest software which is in high demand in market. This training will be designed such that it will useful for their future employment in industry.

STUDENT ASSESSMENT RECORD (SAR)

Record to be maintained by project guide.

1. Project Tools (Hardware/ Software) used fot implementation.

2. Project Evaluation & Execution.

Examination Scheme:

Components	**V**	**S**	**R**	**FP**
Weightage (%)	20	20	20	40

V – Viva, S – Synopsis, FP – Final Presentation, R - Report

Syllabus - Eighth Semester

PROJECT-DISSERTATION

Course Code: ECE2837 **CreditUnits: 08**

Methodology

Topics of project are to be based on the latest trends, verifying engineering concepts /principals and should involve elementary research work. The projects may involve design, fabrications, testing, computer modeling, and analysis of any engineering problem. On completion of the practical training the students are to present a report covering various aspects learnt by them and give a presentation on same.

Guidelines for Project File and Project Report

Research experience is as close to a professional problem-solving activity as anything in the curriculum. It provides exposure to research methodology and an opportunity to work closely with a faculty guide. It usually requires the use of advanced concepts, a variety of experimental techniques, and state-of-the-art instrumentation.

Research is genuine exploration of the unknown that leads to new knowledge which often warrants publication. But whether or not the results of a research project are publishable, the project should be communicated in the form of a research report written by the student.

Sufficient time should be allowed for satisfactory completion of reports, taking into account that initial drafts should be critically analyzed by the faculty guide and corrected by the student at each stage.

Project File

The Project File may be a very useful tool for undertaking an assignment along-with a normal semester, an exploratory study, sponsored projects, a project undertaken during summer period or any other period where the researcher is not working with a company/organization. The project/ assignment may also be a part of the bigger research agenda being pursued by a faculty/ institution/ department

The Project File is the principal means by which the work carried out will be assessed and therefore great care should be taken in its preparation. This file may be considered in continuous assessment.

In general, the File should be comprehensive and include

- A short account of the activities that were undertaken as part of the project;
- A statement about the extent to which the project has achieved its stated objectives;
- A statement about the outcomes of the evaluation and dissemination processes engaged in as part of the project;
- Any activities planned but not yet completed as part of the project, or as a future initiative directly resulting from the project;
- Any problems that have arisen and may be useful to document for future reference.

Project Report

The Project Report is the final research report that the student prepares on the project assigned to him. In case of sponsored project the lay out of the project could be as prescribed by the sponsoring organization. However, in other cases the following components should be included in the project report:

- **Title or Cover Page**
  The title page should contain Project Title; Student's Name; Programme; Year and Semester and Name of the Faculty Guide.
- **Acknowledgement(s)**
  Acknowledgment to any advisory or financial assistance received in the course of work may be given. It is incomplete without student's signature.
- **Abstract**
  A good"Abstract" should be straight to the point; not too descriptive but fully informative. First paragraph should state what was accomplished with regard to the objectives. The abstract does not have to be an entire summary of the project, but rather a concise summary of the scope and results of the project. It should not exceed more than 1000 words.

- **Table of Contents**
  Titles and subtitles are to correspond exactly with those in the text.
- **Introduction**
  Here a brief introduction to the problem that is central to the project and an outline of the structure of the rest of the report should be provided. The introduction should aim to catch the imagination of the reader, so excessive details should be avoided.
- **Materials and Methods**
  This section should aim at experimental designs, materials used (wherever applicable). Methodology should be mentioned in details including modifications undertaken, if any. It includes organization site(s), sample, instruments used with its validation, procedures followed and precautions.
- **Results and Discussion**
  Present results, discuss and compare these with those from other workers, etc. In writing this section, emphasis should be laid on what has been performed and achieved in the course of the work, rather than discuss in detail what is readily available in text books. Avoid abrupt changes in contents from section to section and maintain a lucid flow throughout the thesis. An opening and closing paragraph in every chapter could be included to aid in smooth flow.
  Note that in writing the various secions, all figures and tables should as far as possible be next to the associated text, in the same orientation as the main text, numbered, and given appropriate titles or captions. All major equations should also be numbered and unless it is really necessary, do not write in "point" form.
  While presenting the results, write at length about the the various statistical tools used in the data interpretation. The result interpretation should be simple but full of data and statistical analysis. This data interpretation should be in congruence with the written objectives and the inferences should be drawn on data and not on impression. Avoid writing straight forward conclusion rather, it should lead to generalization of data on the chosen sample.
  Results and its discussion should be supporting/contradicting with the previous research work in the given area. Usually one should not use more than two researches in either case of supporing or contradicting the present case of research.
- **Conclusion(s) & Recommendations**
  A conclusion should be the final section in which the outcome of the work is mentioned briefly.
  Check that your work answers the following questions:
  - Did the research project meet its aims (check back to introduction for stated aims)?
  - What are the main findings of the research?
  - Are there any recommendations?
  - Do you have any conclusion on the research process itself?
- **Implications for Future Research**
  This should bring out further prospects for the study either thrown open by the present work or with the purpose of making it more comprehensive.
- **Appendices**
  The Appendices contain material which is of interest to the reader but not an integral part of the thesis and any problem that have arisen that may be useful to document for future reference.
- **References**
  References should include papers, books etc. referred to in the body of the report. These should be written in the alphabetical order of the author's surname. The titles of journals preferably should not be abbreviated; if they are, abbreviations must comply with an internationally recognised system.
  Examples
  For research article
  Voravuthikunchai SP, Lortheeranuwat A, Ninrprom T, Popaya W, Pongpaichit S, Supawita T. (2002) Antibacterial activity of Thai medicinal plants against enterohaemorrhagic*Escherichia coli* O157: H7. *ClinMicrobiol Infect*, **8** (suppl 1): 116–117.
  For book
  Kowalski,M.(1976) Transduction of effectiveness in *Rhizobium meliloti*. SYMBIOTIC NITROGEN FIXATION PLANTS (editor P.S. Nutman IBP), **7**: 63-67

Layout Guidelines for the Project File & Project Report

- A4 size Paper
- Font: Arial (10 points) or Times New Roman (12 points)

- Line spacing: 1.5
- Top and bottom margins: 1 inch/ 2.5 cm; left and right margins: 1.25 inches/ 3 cm

Assessment of the Project File and the Project Report

Essentially, the assessment will be based on the quality of the report, the technical merit of the project and the project execution. Technical merit attempts to assess the quality and depth of the intellectual efforts put into the project. Project execution is concerned with assessing how much work has been put in.

The Project should fulfill the following assessment objectives:

- Range of Research Methods used to oASEin information
- Execution of Research
- Data Analyses (Analyse Quantitative/ Qualitative information)
- Quality Control
- Conclusions

Assessment Scheme:

Continuous Evaluation:

40% (Based on punctuality, regularity of work, adherence to plan and methodology,refinements/ mid-course corrections etc. as reflected in the Project File.)

Final Evaluation:

60% (Based on the Documentation in the file, Final report layout, analysis andresults, achievement of objectives, presentation/ viva)

Examination Scheme:

Literature study/ Fabrication/ Experimentation	40
Written Report	20
Viva	15
Presentation	25

INSTRUMENTATION

Course Code: ECE2803 **CreditUnits: 03**

Course Objective:
The basic objective of this course is to provide the students the core knowledge of industrial instrumentation so that they learn how to implement instrumentation techniques in industry.

Course Contents:

Module I: Introduction to Measurement & Instrumentation
Classification, Characteristics of measuring instruments: accuracy, precision, error, linearity, hysteresis, resolution & sensitivity, generalized instrumentation systems, primary sensing elements-definition & examples, transducers: definition & Classification; measurement of pressure- diaphragms, capsules, bourdon tubes, strain-gauge transducers, LVDT type, Temperature Measurement (RTD, Thermocouple , thermistor, optical pyrometer); Measurement of force:-load cell(column type, proving ring, shear type), Measurement of flow classification flow meters, head type flow meters-Venturi tube, flow nozzle, pitot tube

Module II: A. C. Instruments
A.C. Voltmeter using rectifier; True RMS responding Voltmeter; Electronics Multimeter; Digital Voltmeter; spectrum analyzer, harmonic distortion analyzer, CRO-introduction, construction of conventional CRO. Digital storage oscilloscope.

Module III: Telemetry
Telemetry-introduction & different types of telemetry system, data acquisitions-signal conditioning, single channel & multichannel data acquisition system.

Module IV: Miscellaneous Instruments
Computer controlled test systems-introduction, testing of audio amplifier, Testing of Radio Receiver; Instruments used in computer controlled instrumentation, IEEE 488 electrical interface, Fiber optic Instrumentation.

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

Text:

- A. K. Sawhney, 2005, "Measurement & Instrumentation" Dhanpat Rai Publications.
- Rangan, Sarma, Mani, "Instrumentation- devices&systems", TMH
- Helfrick, Cooper, "Modern Electronic Instrumentation & Measurement Techniques", PHI – 4th Reprint.

References:

- Johnson, "Process Control Instrumentation" PHI – 7th Edition

RTOS PROGRAMMING

Course Code: ECE2805 **CreditUnits: 03**

Course Objective:

RTOS stands for Real Time Operating System

The syllabus is divided into five modules, the first one deal with RTOS basic concepts and its features like scheduling and its interrupt routines environment. Second module include in depth detail of dynamic and the Static-priority scheduling with Practical considerations. Module 3 deals with concepts like Resource sharing, Priority and stack resource protocols. A basic Overview of operating Systems is also covered. Module 4 and 5 looks various available commercial real-time and non-real-time operating systems and there Porting on microcontroller based development system board along with of Linux, Shell and RT Linux programming.

The syllabus makes student perfect in RTOS concepts like scheduling and sharing tasks apart from it Linux programming is discussed in detail.

Course Contents:

Module I: Introduction and basic concept

Introduction to real-time, Example real-time applications, Hard vs. soft real time., OS Services, I/O Subsystems, Interrupt Routines in RTOS Environment, RTOS Task Scheduling model, Interrupt Latency and Response times of the tasks. Reference model.

Module II: Itatic and dynamic scheduling

Classic uniprocessor scheduling, Static scheduling, dynamic scheduling, Dynamic-priority scheduling, Static-priority scheduling, Dealing with Complexities arising in real systems, Practical considerations.

Module III: sharing, protocols and real time systems

Resource sharing, Priority inheritance and priority ceiling protocols, stack resource protocol. systems A quick look at some real systems ,Basic operating-system functions needed for real-time computing, Overview of operating Systems.

Module IV: Operating systems and embedded systems

A brief survey of commercial real-time and non-real-time operating systems: Embedded OS, Real Time OS, Hand held OS, Porting RTOS on a Microcontroller based development system board.

Module V: Shell and RT LINUX programming

Programming in Linux, Shell programming, System Programming,
Programming in RT Linux

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

Text:

- Embedded systems, Raj Kamal, TMH
- Real-Time Systems, Jane W. S. Liu, , Prentice-Hall, Inc 32
- David E. Simon, "An Embedded Software Primer",
- Pearson Education, 1999.

References:

- Embedded system design: An Introduction to processes tools & Techniques, A.S. Berger, CMP
- Books.
- Dr. Prasad, "Embedded Real Time System", Wiley Dreamtech, 2004.

VERILOG PROGRAMMING

Course Code: ECE2806 **CreditUnits: 02**

Course Objective:
This course discuss fundamental Verilog concepts of today's most advanced digital design techniques. it offers broad coverage of Verilog HDL from a practical design perspective. Introduces students to gate, dataflow (RTL), behavioural, and switch level modeling, describes leading logic synthesis methodologies; explains timing and delay simulation; and introduces many other essential techniques for creating tomorrows complex digital designs

Course Contents:

Module I: Introduction to Verilog HDL and Basic Concepts
Emergence of HDL, typical design flow, trends in HDL, Modeling concept
Design methodologies, modules, instances, simulation, design block and stimulus block
Lexical conventions, Data Types. System Tasks and Compiler Directives, Modules and Ports

Module II: Gate-Level Modeling and Dataflow Modeling
Gate Types. Gate Delays, Continuous Assignments. Delays. Expressions, Operators, and Operands. Operator Types. Examples for combinational and sequential circuit using Gate level and Data-flow modeling

Module III: Behavioural Modeling
Structured Procedures. Procedural Assignments. Timing Controls. Conditional Statements. Multiway Branching. Loops. Sequential and Parallel Blocks. Generate Blocks. Examples

Module IV: Tasks and Functions and Useful Modeling Techniques
Difference between Tasks and Functions. Tasks. Functions.
Procedural Continuous Assignments. Overriding Parameters. Conditional Compilation and Execution. Time Scales. Useful System Tasks

Module V: Advanced Verilog Topics
Timing and Delays. Switch Level Modeling,User-Defined Primitives, Logic Synthesis with Verilog HDL, Advanced Verification Techniques

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

- Samir Palnitkar, “Verilog HDL”, Pearson Education (2nd edition).
- Donald Thomas, Philip moorby, “The Verilog hardware Description language” 5th Edition, Kluwer Academic publishers
- VivekSagdeo,” The Complete Verilog Book”
- Parag K. Lala, Self-Checking and Fault-Tolerant Digital Design , Academic Press
- J. Bhasker, Verilog HDL Synthesis: A Practical Primer,1998

VERILOG PROGRAMMING LAB

Course Code: ECE2813 **CreditUnits: 01**

List of Experiments

- Write a Verilog code to realize all the logic gates.
- Write a Verilog code to implement Half Adders, Full adders and Subtracters using Gates.
- Write a Verilog code to describe the function of Multiplexer and Demultiplexer using different modelling styles.
- Write a Verilog code to realize D Flip-Flop and D Latch.
- Write a Verilog code to implement 2:1 Mux and D Latch using Switches.
- Write a Verilog code to implement Encoders and Decoders Using if-else Statement and case Statement.
- Write a Verilog code to implement SR Flip Flop using UDP (User Defined Program).
- Write the Verilog code for a JK Flip-flop, and its test bench. Use all possible combinations of inputs to test its working.
- Write the hardware description of a 8-bit register with parallel load, shift left and shift right modes of operation and test its operation.
- Write a Verilog code to realize Up/Down Counter and Divide by 4.5 Counter. Write a Verilog code to describe the function of Synchronous FIFO.
- Write a Verilog code using FSM to realize a sequence detector (101101).

Examination Scheme:

IA				EE	
A	**PR**	**LR**	**V**	**PR**	**V**
5	10	10	5	35	35

Note: IA –Internal Assessment, EE- External Exam, PR- Performance, LR – Lab Record, V – Viva.

ADVANCED NETWORKING

Course Code: ECE2807 **CreditUnits: 03**

Course Objective:
The objective here is to acquaint the students with the application of networking. Detail description of the various TCP/IP protocols and the working of ATM and its performance, Network security and authentication, and various algorithms related to it has been dealt, to get a practical approach.

Course Contents:

Module I: TCP/IP Protocol
Layered protocols, internet Addressing, mapping internet address to physical address, internet protocol, OSPF, RIP, RARP, BOOTP, DHCP, BGP, ARP, IP, Ipv6, ICMP
Transport protocols: UDP, TCP, SNMP

Module II: Connection oriented networks
Frame relay, B-ISDN, ATM protocol stack, ATM switching, internetworking with ATM Networks, traffic management in ATM.

Module III: High Speed LAN
LAN Ethernet, fast Ethernet, gigabit Ethernet, FDDI,
DSL, ADSL

Module IV: Wireless communication
Wireless networks, wireless channels, channel access, network architecture, IEEE 802.11, bluetooth

Module V
Network Analysis And Modeling: Queuing theory, modeling network as a graph, network management system and standard

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
Text:
- High performance communication networks by: J. Walrand& Pravin Varaiya , Morgan Kaufman, 1999.
- Internetworking with TCP/IP Vol.1: Principles, Protocols, and Architecture (4th Edition) by Douglas E. Comer
- ATM networks: Concepts, Protocols, Applications by: Handel, AddisionWesseley.
- Cryptography & Networks Security Stallings, William 3rd edition

References:
- Computer networks:Tanenbaum, Andrew S, Prentice Hall
- Data communication & networking: Forouzan, B. A.
- Computer network protocol standard and interface Uyless, Black

ADVANCED VLSI DESIGN

Course Code: ECE2812 **CreditUnits: 03**

Course Objective:
This is advanced Analog design based course which will lay strong foundation in this direction for students seriously interested in making a career as an Analog Designer.

Course Contents:

Module I: Review of Elementary transistor stages
MOST single transistor amplifying phase, BJT single transistor, Source and emitter follower and their noise performance, Cascade transistors and noise performance

Module II: Inverter stage and Building Blocks
CMOS inverter, DC analysis, low frequency gain, bandwidth, current capacity, slew rate, amplifying phase, BJT inverter stage and Noise performance, Cascade and its Bandwidth, active load, differential stages, current mirrors and their noise output

Module III: Op amp Design: Introduction
Design of single transistor OTA: GBW and phase margin, Miller CMOS OTA: GBW and phase margin, Full Dc analysis: Common mode input voltage range versus current supply, output range versus supply voltage, maximum output current, source and sink, Noise analysis of OTAs

Module IV: Op amp Design: Matching specifications
Transistor mismatch, Offset voltage definition, Mismatch definition, differential stage with active load, Offset drift, CMRR, Offset and CMRR of Miller OTA, Offset in BJT and JFET, Power Supply rejection ratio of simple and Miller OTA

Module V: Design of OTAs and design Options
Symmetrical, Cascade OTA, Folded Cascade OTA, Operational Current Amplifier, design for optimum GBW and SR, CMOS Configurations, Bipolar op amp configurations

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:
- Laker and Sansen: Design of Integrated Circuits
- Gray, Hurst, Lewis and Meyer: Analysis and design of Analog ICs
- Razavi Design of Analog CMOS Integrated Circuits

POWER ELECTRONICS

Course Code: ECE2814 **CreditUnits: 03**

Course Objective:
The course aims to introduce them to the theory of operation, analytical and circuit models and basic design concepts of Electric Power components and systems.

Course Contents:
Module I: Triggering Devices
Triggering devices, Unijunction Transistor, Characteristics and applications of UJT, Programmable Unijunction Transistor, DIAC, Silicon Controlled Switch, Silicon Unilateral Switch, silicon Silicon bilateral Switch, Shockley diode.

Module II: Thyristor Firing Circuits, Turn on systems
Two transistor model of Thyristor, Method of Triggering a thyristor, Thyristor Types, Requirement for triggering circuits, Thyristor Firing Circuits, Fullwave control of Ac with one thryristor, Light activated SCrs (LASCR), Control Circuit, dv/dt and di/dt protection of Thyristor, Pulse Transformer triggering, Firing SCR by UJT, TRIAC firing circuit, Phase control of SCR by pedestal and Ramp.

Module III: Controlled Rectifiers
Types of Converters, effect of inductive load, Commutating diode or free wheeling diode, controlled rectifiers, Bi phase half wave, single phase full wave phase controlled converter using bridge principle, harmonics.

Module IV: Inverters
Types of Inverters, Bridge Inverters, Voltage Source Inverters, Pulse Width Modulation Inverters, Current source Inverters.

Module V: AC Voltage Controllers
Types of AC voltage Controllers, AC Phase Voltage controllers, single Phase Voltage Controller with RL load, harmonic analysis of single phase full wave controller with RL load.

Module VI: DC to DC Converters
DC choppers, Chopper classification, two quadrant chopper, Four quadrant chopper.

Module VII: Cycloconverter
Single phase and three phase cycloconverters.

Module VIII: Industrial Applications
One shot Thyristor trigger Circuit, over voltage protection, simple battery charger, battery charging regulator, AC static switches, DC static switch

Examination Scheme:

Components	A	CT	S/V/Q	HA	EE
Weightage (%)	5	10	8	7	70

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; Att: Attendance

Text & References:

Text:

- J. Michael: Power Electronics: Principles and Applications
- M. H. Rashid: Power Electronics circuits

References:

- H. C. Rai, "Power Electronics Devices, Circuits, Systems and Application", Galgotia, 3rd Ed.
- P. S. Bimbhara, "Electrical Machinery, Theory Performance and Applications" Khanna Publications, 7th Ed